

A Novel Nanometric Parity Preserving Reversible Vedic Multiplier

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ABSTRACT

Reversible computation is an emerging area of research, having applications in nanotechnology, low power design and quantum computing. It is proved that reversible logic has zero internal power dissipation. Multiplication plays an important role in the processors. It is one of the basic arithmetic operations and it requires more hardware resources and processing time than the other arithmetic operations. Vedic mathematic is the ancient Indian system of mathematic. It has a unique technique of calculations based on 16 Sutras. The multiplication sutra between these 16 sutras is the Urdhva Tiryakbhyam sutra which means vertical and crosswise. In this paper it is used for designing a novel Nanometric parity preserving 4*4 reversible Vedic multiplier. The important parameters in designing reversible logic circuits like quantum cost, number of constant inputs and number of garbage outputs are estimated and reported for our proposed parity preserving reversible Vedic multiplier. All the scales are in the Nanometric area whose fundamental parts are no bigger than a few nanometers.

KEYWORDS: Nanometric Circuits, Nanotechnology, Quantum Computation, Vedic Multiplier, Urdhva Tiryakbhyam sutra, Parity Preservation, Reversible Logic, Nanoscale Technology.

1- INTRODUCTION

Irreversible circuits have internal power dissipation regardless of their realization techniques [1]. This is due to the information loss during the computations. It is proved that for every bit of information that is lost during a computation, $KT\ln 2$ Joules of energy dissipates, where $K=1.3806505 \times 10^{-23} \text{ m}^2 \text{ kg}^{-2} \text{ K}^{-1}$ (Joules/Kelvin) is the Boltzmann's constant and T is the absolute [2]. Reversible logic design has the advantage of theoretically zero internal power dissipation because those circuits do not lose information. As the reversible logic circuits have zero internal power dissipation, they are of interest in many areas such as low power design and quantum computation [3].

A circuit is reversible if and only if the number of input lines and the number of output lines are equal and it maps each input pattern to a unique output pattern. Such circuits allow the reproduction of the inputs from observed outputs and we can determine the inputs from the outputs [3][4][5][6].

The quantum cost (QC) of a reversible circuit is defined as the number of 1×1 or 2×2 gates used to implement the reversible circuit [3][6]. Reversible circuits have some restrictions:

- Feedback is not allowed in reversible circuits.
- Fan-out is forbidden in reversible logic.

Some factors such as the amount of garbage outputs, the number of constant inputs and the quantum cost (QC) are very important parameters in reversible logic design. We try to minimize all of these parameters [3][5][7][8][9].

If a Nanometric system is made up of fault tolerant components, then it will be able to continue operating properly when the failure occurs in some of its components [6]. Fault tolerance can be achieved by using parity bits. Thus, parity preserving reversible circuit design is important for development of Nanometric fault tolerant reversible systems in nanotechnology [10][6].

There exist several multiplication methods. Vedic mathematic is the ancient Indian system of mathematic. It has a unique technique of calculations based on 16 Sutras. The multiplication sutra between these 16 sutras is the Urdhva Tiryakbhyam sutra which means vertical and crosswise.

In this paper we propose a novel Nanometric parity preserving reversible Vedic multiplier. The above mentioned complexity factors are estimated and reported for our proposed Nanometric parity preserving reversible Vedic multiplier.

The organization of the paper is as follows: Section 2 covers the basic concepts including reversible logic gates, parity preserving reversible gates and an overview of Vedic mathematics especially Vedic multiplier. Our proposed Nanometric parity preserving reversible Vedic multiplier is presented in section 3. Conclusions and references are in sections 4 and 5, respectively.

2. Basic Concepts

In this section brief background about Nanometric reversible logic gates, parity preserving reversible logic gates and Vedic multiplier is presented. It is to be noted that only required and related reversible logic gates and circuits are explained.

Reversible Logic Gates: A gate or a circuit is reversible if and only if the number of input lines and the number of output lines are equal and it maps each input pattern to a unique output pattern. Such circuits allow the reproduction of the inputs from observed outputs and we can determine the inputs from the outputs [3][4][5][6][11]. There are many reversible logic gates. Among them, 2×2 Feynman Gate [12] is depicted in Fig. 1.a. It implements the logic functions: $P=A$, and $Q=A \oplus B$. Feynman gate is also known as controlled NOT (1-CNOT). It can act as a BUFFER gate if the control input is set to $A=0$. Feynman gate can also act as a NOT gate if the control input is set to $A=1$. The Feynman gate can be used as fan-out gate to provide a copy of a single bit because the fan-out is not allowed in the reversible circuits. If the B input in Fig.1.a is set to $B=0$ then both outputs of the Feynman gate are equal to the input A .

Toffoli [13] and Peres [14] gates are 3×3 reversible gates which are depicted in Fig.1.b and Fig.1.c respectively. Both of them are universal gates. That is, any logical circuit can be implemented using each of these reversible logic gates. The Feynman gate is a one-through gate, i.e. one of the input lines is also output. The Peres gate is also a one-through gate. Toffoli gate (Fig.1.b) is two-through gate, i.e. two of the input lines are also outputs.

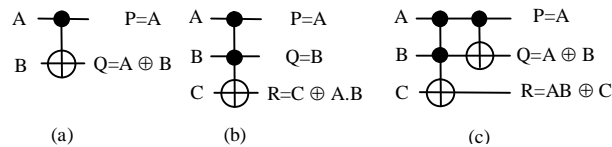


Fig.1 Reversible logic gates (a) Feynman gate (b) Toffoli gate (c) Peres gate

As Toffoli gate is a two-through gate, it has two control inputs that are copied to the first two outputs. The last input of the Toffoli gate is complemented if both control inputs are 1's and is directly copied to the last output, otherwise.

Peres gate (PG), also known as NTG can work as a Toffoli gate followed by a Feynman gate [9]. The Peres gate is depicted in Fig.1.c.

Quantum Cost: The quantum cost (QC) of a reversible logic gate or circuit is defined as the number of 1×1 or 2×2 quantum gates, needed to implement the gate or circuit. The QC of the Feynman gate is 1. The QC of the Toffoli gate is 5 and the QC of the Peres gate is only 4.

Constant input: Constant input is the input that its value is fixed to be either '0' or '1' [3].

Garbage Output: Garbage Output refers to the output that is neither used as primary output nor for further computations, but it is added to make the circuit reversible [3]

Parity Preserving Reversible Gates: Parity preserving reversible gates or circuits are those gates or circuits which their input and output parities are the same. Most of arithmetic and other processing functions do not preserve the parity of the input data in the output. Parity checking is one of the most widely used methods for error detection in digital logic systems [15][16][6]. Therefore it is important to design parity preserving reversible circuits.

There are many reversible logic gates but only a few of them preserve the parity. The Fredkin gate [17] (FRG) which is depicted in Fig. 2 is a parity preserving reversible gate. The F2G [18] gate depicted in Fig.3, the NFT gate depicted in Fig 4, and the IG gate which is depicted in Fig.5 are also parity preserving reversible gates. These gates are parity preserving gates because their input parity is the same as their output parity. The Qc of FRG is only 5. The QC of F2G is only 2. The QC of NFT and IG are 5 and 7 respectively.

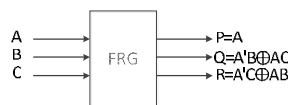


Fig.2 Parity Preserving Reversible Fredkin gate. Its QC is only 5.

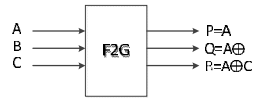


Fig.3 Parity Preserving Reversible F2G gate. Its QC is only 2.

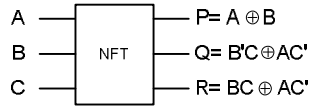


Fig.4 Parity preserving reversible NFT gate. Its QC is only 5.

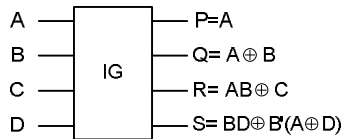


Fig.5 Parity preserving reversible IG gate. Its QC is only 7

Vedic Multiplier: Vedic mathematic is the ancient Indian system of mathematic. It has a unique technique of calculations based on 16 Sutras. The multiplication sutra between these 16 sutras is the Urdhva Tiryakbhyam sutra which means vertical and crosswise. In this paper it is used for designing a novel Nanometric parity preserving reversible Vedic multiplier. This is to be noted that the authors in [19] suggested a reversible 8*8 Vedic multiplier based on Nikhilam sutra of ancient Vedic Mathematics. Nikhilam sutra can only perform efficient multiplication of numbers nearer to base 100 [19][20]. Hence we do not use Nikhilam sutra. Instead of that, we use Urdhva Tiryakbhyam sutra.

Urdhva-Tiryagbhyam sutra is a general formula which is applicable to all the multiplication operations. Algebraic principle of Urdhva-Tiryagbhyam sutra is based on multiplication of polynomials [21]. The Vedic multiplier using Urdhva-tiryagbhyam sutra of width $N \times N$ will generate the $2N-1$ cross products of different widths and forms $(\log_2 N + 1)$ partial products. The partial products are obtained by vertical and crosswise operations. Thus the delay is the same as adder delay. The Critical path would consist of adders adding the maximum number of bits in cross product [21]. Fig. 6 represents the general multiplication procedure of the 2×2 multiplication using Urdhva-Tiryagbhyam sutra. The algorithm can be generalized for $n \times n$ bit numbers. Fig. 7 represents the multiplication procedure of the 4×4 vedic multiplier using 2×2 multiplication.

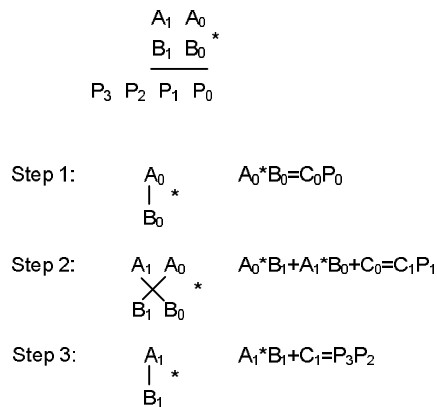


Fig.6. Structure of 2×2 Vedic Multiplier

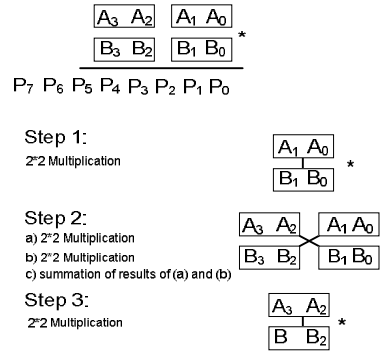


Fig.7. Structure of 4*4 Vedic Multiplier. In this structure we use 2*2 Multiplier to multiply the 2-bit blocks.

3. Our Proposed Parity Preserving 4*4 Reversible Vedic Multiplier Structure

In this section we propose a novel parity preserving 4*4 reversible Vedic multiplier. The proposed circuit is depicted in Fig. 8. The circuit consists of:

1. Eight F2G gates.
2. Three parity preserving reversible 4-bit adders.
3. Four parity preserving reversible 2*2 multipliers.

The structure of the Parity Preserving Reversible 4 bit adder is depicted in Fig. 9.a. It consists of 8 IG gates. Thus its QC is $8*7=56$. The proposed parity preserving reversible 2*2 multiplier is depicted in Fig. 10. Its QC is 42.

The QC of the proposed parity preserving 4*4 reversible vedic multiplier is the sum of these parts:

1. QC of eight F2G gates is 16.
2. The quantum cost of the three parity preserving reversible 4-bit adders is $3*56=168$.
3. The quantum cost of the four parity preserving reversible 2*2 multipliers is $4*42=168$.

Thus the QC of the proposed parity preserving 4*4 reversible vedic multiplier is $16+168+168=352$.

Specifications of our proposed parity preserving reversible 4*4 vedic multiplier is depicted in Table 1.

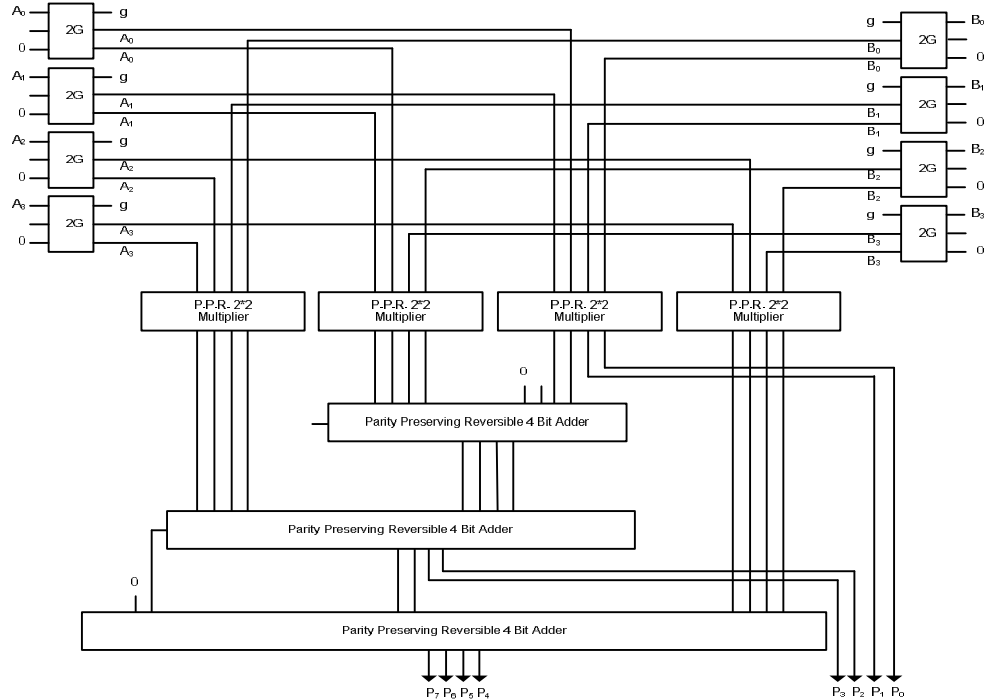


Fig.8. Our proposed Parity Preserving Reversible 4*4 Vedic Multiplier Structure.

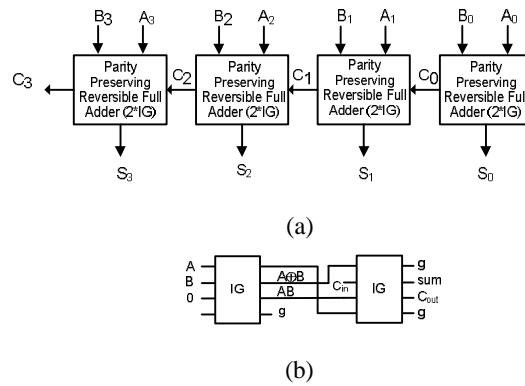


Fig.9. (a) Parity Preserving Reversible 4 bit adder. Its QC is 56. (b) Parity Preserving Reversible full adder (2* IG). Its QC is 14.

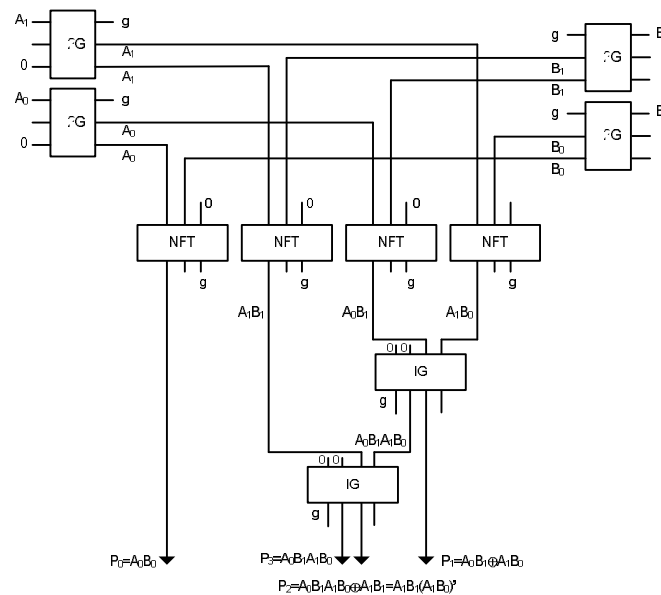


Fig.10. Our proposed Parity Preserving Reversible 2*2 Multiplier. Its QC is 42.

Table 1: Specifications of our proposed Nanometric parity preserving reversible 4*4 vedic multiplier

Design	No. of Garbage Outputs	Quantum Cost	No. of Constant Inputs
Our proposed Nanometric parity preserving reversible 4*4 vedic multiplier	110	352	102

4. Conclusions

Multiplication plays important role in the processors. Reversible computation is an emerging area of research, having applications in nanotechnology. It is proved that reversible logic has zero internal power dissipation. In this paper a novel Nanometric parity preserving reversible Vedic multiplier is proposed using Urdhva Tiryakbhyam sutra. The quantum cost, number of constant inputs and number of garbage outputs of all its blocks and the whole circuit are reported. All the scales are in the Nanometric area whose fundamental parts are no bigger than a few nanometers.

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