J. Basic. Appl. Sci. Res., 3(6)732-735, 2013
© 2013, TextRoad Publication

ISSN 2090-4304
Journal of Basic and Applied Scientific Research
www.textroad.com

An Improvement in the Differential Mode Gain of a single-output CMOS Differential Amplifier with an Active Load

Mostafa Bijani[1], Mahmoud Aleshams[2]

[1]Department of Electrical Engineering, Boushehr Branch, Islamic Azad University, Boushehr, Iran
[2]Department of Electrical Engineering, Fasa Branch, Islamic Azad University, Fars, Iran

ABSTRACT

A single-output CMOS differential amplifier is one of useful analog building blocks for signal-processing applications in mixed-signal circuits. One of advantages of using a differential amplifier instead of other transistor amplifiers is its simple biasing and high amplifier gain. In this paper, in order to improve the differential mode gain, we propose a design for a single-output CMOS differential amplifier with an active load. This circuit can reach a differential-mode gain of 165 while consuming power of 195 μw.
KEYWORDS: differential mode gain, differential amplifier, active load.

INTRODUCTION

Among basic analog circuits, a single-output differential amplifier with an active load plays an essential role. This is due to its good performance as the input stage [1]-[3]. Figure 1 shows a circuit model for a voltage amplifier. This model includes a voltage-controlled voltage source with gain A_{v0}, an input resistance R_i , and an output resistance R_o. The input resistance determines the amount of the current taken from the signal source while, the output resistance shows the output voltage change due to the current taken by the load. Then voltage gain of the voltage amplifier, then is given by

$$A_v = \frac{V_o}{V_i} = A_{vo}\frac{R_i}{R_i + R_o} \qquad (1)$$

In order to avoid gain loss when coupling the amplifier's output to a load, output resistance R_o must be greatly smaller than the load resistance R_L. Such a condition can be seen in a differential amplifier with an active load. So far, different topologies for a differential amplifier with an active load and a single-output have been proposed [4]-[6], but one of the most attractive designs for this kind amplifier has been presented in [6]. This circuit has many capabilities in the field of self-biasing, common mode rejection, and bandwidth. However, in this paper we propose a new design for the differential amplifier with an active load and a single-output giving more differential mode gain rather than this circuit.

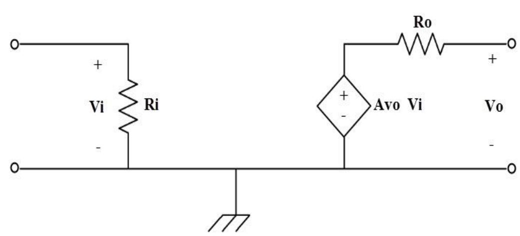

Fig. 1. A circuit model for a voltage amplifier.

MATERIAL AND METHODS

The differential amplifier with an active load and a single output due to [6] is shown in Fig. 2. In this circuit M_1 and M_2 are two equal input transistors to amplify the input signal, M_3 and M_4 play the role of an active load, while M_5, M_6, and R_1 act as a current source. The differential mode gain for this amplifier is calculated based on its small signal model illustrated in Fig. 3, where each g_{mi} and r_{di} are the trans-conductance and the drain resistance related to transistor M_i, respectively. Since we can generally suppose that $r_{d1} > \frac{1}{g_{m3}}$, then the current passing through r_{d1} is negligible and we can derive the differential mode gain of the circuit as:

*Corresponding Author: Mostafa Bijani, Department of Electrical Engineering, Boushehr Branch, Islamic Azad University, Boushehr, Iran. Email: s_m_bijani@yahoo.com

$$A_{vd} = \frac{V_o}{V_d} = -g_{m1,2}(r_{d2} \| r_{d4}) \qquad (2)$$

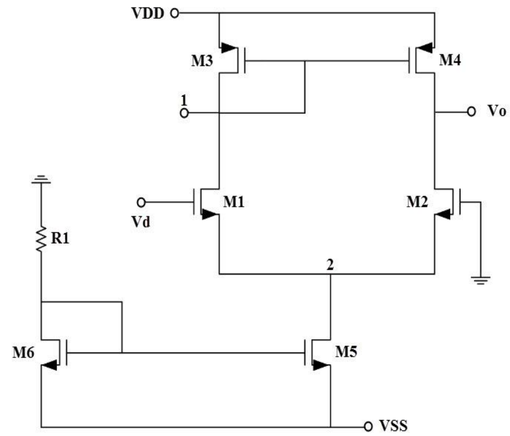

Fig. 2. A differential amplifier with an active load and a single-ended output [6].

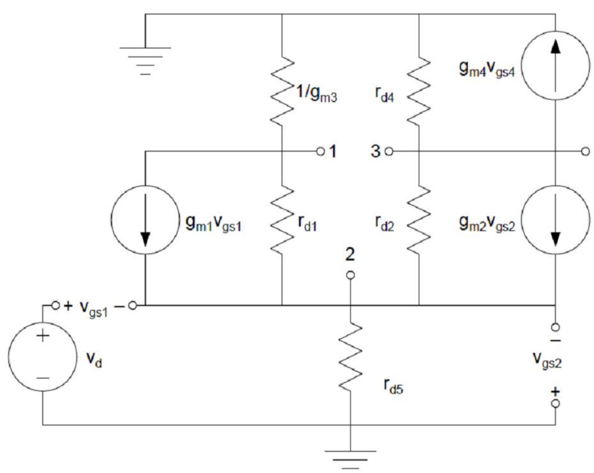

Fig. 3. An equivalent small-signal circuit for the differential amplifier with an active load and a single output shown in Fig. 2.

Our proposed circuit for a differential amplifier with an active load and a single output is based on the above mentioned circuit and is shown in Fig. 4. In this design, there are some modifications for the current source, and the active load. The small-signal equivalent model for this circuit is shown in Fig. 5.

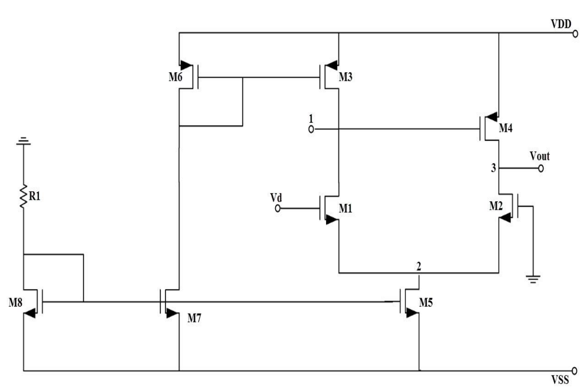

Fig. 4. Our proposed single-output differential amplifier with an active load.

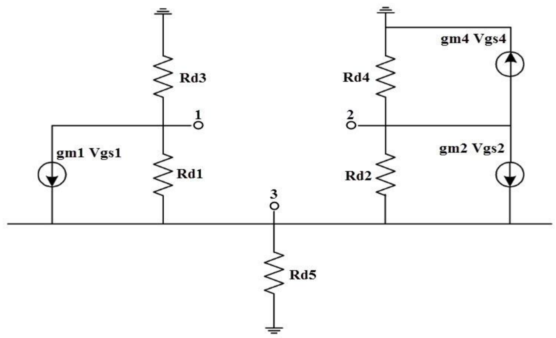

Fig. 5. An equivalent small-signal circuit for the new differential amplifier.

RESULTS AND DISCUSSION

Using the 0.25 µm process and the parameters due to the SPICE BSIM, all transistors' channel lengths are taken 1µm, while the channel widths for all NMOS and PMOS transistors are chosen 4.5 and 18.5 µm, respectively. Besides, we assume the voltages for both power supplies to be 2.5 V and the resistance R_1 equal to 102 KΩ. By applying a sinusoidal differential input signal with the amplitude 1mV, the amplification of the signal for both circuits shown in Fig. 2 and Fig. 4 are illustrated in Fig. 6 and Fig. 7, respectively. Also the differential mode gain and the total power consumed, P_{diss} in each circuit are given in Table I. As we see from this Table, the differential mode gain is significantly increased for our proposed circuit, although as a disadvantage the dissipation power is also increased.

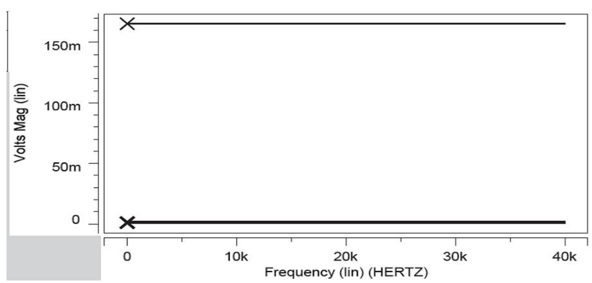

Fig. 6. The amplification of the input differential signal for the differential amplifier presented in [6].

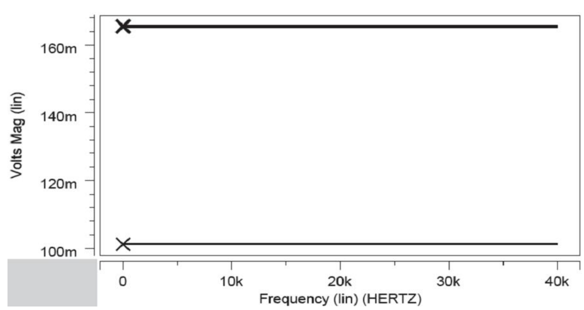

Fig. 7. The amplification of the input differential signal for the differential amplifier proposed in this paper.

Table I. The simulation results

Parameters	The diff. amplifier due to [6]	Our proposed circuit
A_V	101	165
P_{diss} (μw)	145	195

CONCLUSIONS

A single-output CMOS differential amplifier is attractive as one of useful analog building blocks for signal-processing applications in mixed-signal circuits. In this paper a new single-output differential amplifier with an active load is proposed so that in many applications which differential mode gain has more important role than total power consumption in circuit, we can use it in place of other similar circuits such as that presented in [6].

REFERENCES

[1] Sedra, A. S., and K. C. Smith, 1998. Microelectronic Circuits, 4'h ed ,.Oxford University Press.

[2] Gray, P. R., P. J. Hurst, S. H. Lewis and R. G. Meyer, 2001. Analysis andDesign of Analog Integrated Circuits, 4'th ed., John Wiley & Sons.

[3] Razavi, B., 2002. Design of Analog CMOS Integrated Circuits, New York: McGraw Hill Companies Inc.

[4] Corsi, F., and C. Marzocca, 2003. An Approach to the Analysis of theCMOS Differential Stage with Active Load and Single-EndedOutput: IEEE Trans. Educ., 46: 325-328.

[5] Dhali, S. K, 1999. Analysis of the Differential Amplifier with an ActiveLoad: IEEE Trans. Educ., 42: 295-304..

[6] Butkovic, Z., and A. Szabo, 2004. Analysis of CMOS Differential Amplifier with Active Load and Single-ended Output: IEEE MELECON, 1: 417 – 420.