

Designing a Novel Nanometric Parity Preserving Reversible ALU

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ABSTRACT

Reversible logic circuits have a vital role in nanotechnology-based systems, quantum computing, low power CMOS design, optical information processing and bioinformatics. The role of computational nanotechnology has become considerable in the nanotechnology development. In this paper, we propose a novel nanometric reversible ALU which uses parity preserving reversible gates as its basic building blocks. The parity preserving reversible gates are those gates that allow any fault that affects no more than a single signal to be detectable at the circuit primary outputs. The proposed parity preserving reversible ALU is optimized in terms of quantum cost, the number of garbage outputs, the number of constant inputs and hardware complexity. It can be used to construct more complex systems in nanotechnology. All the scales are in the nanometric area.

KEYWORDS: Reversible logic, fault tolerant, nanometric circuits, Arithmetic Logic Unit, parity preserve.

1. INTRODUCTION

Parity checking is one of the widely used error detection mechanisms in digital logic and data communication systems. Therefore, parity-preserving reversible circuits will be the future design trends towards the development of fault tolerant reversible systems in nanotechnology. A sufficient requirement for parity preservation of a reversible circuit is that each gate be parity preserving [1]. Thus, we need parity preserving reversible logic gates to construct parity preserving reversible circuits. In parity preserving logic gate, the parity of the inputs must match that of the outputs [6-7].

Reduction of power dissipation is one of the important aims in the nanoscale design of circuits. According to R.Landauer's researches in the early 1960s, the amount of energy (heat) dissipated for every irreversible bit operation is given by KTln2, where K = 1.3806505*10-23JK-1 is the Boltzmann constant and T is the operating temperature [2]. In 1973, Bennett showed that in order to avoid KTln2 joules of energy dissipation in a circuit, it must be built using reversible logic gates [3].

Reversible logic circuits have theoretically zero internal power dissipation because they do not lose information. Neither feedback (loop) nor fan-out is permitted in reversible logic circuits [12]. Thus, the synthesis of quantum or reversible logic circuit is significantly more complicated than traditional irreversible logic circuits. It is also more difficult to make a parity preserving reversible circuit than a conventional logic circuit. In this paper an efficient parity preserving reversible ALU is presented [5].

Since the Arithmetic Logic Unit (ALU) is one of the essential components of the Central Processors, its well performance is the most important factor in obtaining the high reliability. The reversible logic has also found as emerging attention in nanotechnology, optical computing, quantum computing and low power CMOS design [11].

Basic concepts of reversible logic gates are given in Sec. 2. The proposed parity preserving reversible ALU circuit is presented in Sec. 3. Evaluation of the proposed circuit is presented in Sec. 4. Conclusion is presented in Sec. 5. A comprehensive list of references is also provided.

2. Basic Concepts

In this section, we review the reversible logic gates used in this paper and how logical operations can be achieved from these gates [5]. Several reversible logic gates have been proposed in the past years. Some of them are like Feynman Gate, FG [9], Feynman Double Gate, F2G [1], Fredkin gate, FRG [4], NFT gate [5] and IG gate [6-7]. All of the aforementioned gates except FG are parity preserving and are used in our implementation.

Reversible logic: an "n" input and "n" output function 'F', is reversible if there is one to one correspondence between inputs and outputs. Therefore we can determine the input vector from output vector uniquely [10].

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Quantum cost: Number of 1 * 1 or 2 * 2 reversible logic gates which are needed to make the reversible circuit is called quantum cost (QC).

Constant inputs: The inputs that are added to an n * k function to make it reversible are called constant inputs [8].

Garbage output: If the output of gate is not used for further computation, this output is called garbage output [11]. **Parity preserving reversible gate:** If parity of inputs and parity of outputs are equal in reversible gate, this gate is called parity preserve. Reversible gate is "fault tolerant" if it is parity preserve.

Conservative gate: A gate is conservative if the hamming weight of its input vector is the same as the Hamming weight of its output vector [11].

Feynman Gate (FG): Feynman gate also known as controlled-not gate (CNOT), is a 2*2 reversible gate that can be describe by the equations: P = A, and $Q = A \oplus B$, where "A" is control bit and "B" is the target bit. It is shown in Fig. 1. The Feynman gate can be used to copy a signal. If the B input in Fig. 1 is "0" then both of the outputs will be equal to A. Since fan-out is not allowed in reversible logic circuits, the Feynman gate is used as the fan-out gate to copy a signal. The QC of this gate is one.



a. Block diagram

b. Quantum implementation

Fig 1. 2*2 Reversible Feynman gate

Feynman Double Gate (F2G): Let $I_v = (A, B, C)$ and $Q_v = (P = A, Q = A \oplus B, R = A \oplus C)$ be the input and output vectors of a 3*3 Feynman Double Gate, (F2G). The F2G is a Feynman Gate with an extra input and one more output. Feynman Double Gate can also be used as the fan-out gate. It is depicted in Fig. 2. This gate is parity preserving and has a OC of 2 [1].

Fredkin gate (FRG): Fredkin gate, also known as controlled permutation gate is a 3*3 reversible logic gate. It can be represented as:

$$I_{v} = (A, B, C)$$
$$Q_{v} = (P = A, Q = AB \oplus AC, R = AC \oplus AB)$$

Where I_{ν} and Q_{ν} are input and output vectors. It is shown in Fig. 3. Fredkin gate is a conservative gate and parity preserving too. This gate has a QC of 5.



b. Quantum implementation

Fig 2. 3*3 Reversible Feynman Double gate



a. Block diagram

b. Quantum implementation

Fig 3. 3*3 Reversible Fredkin gate

IG gate: IG gate is a 4*4 reversible logic gate. IG gate has a QC of 7. It can be represented as:

$$I_{v}$$
=(A,B,C,D)

$$Q_{v} = (P = A, Q = A \oplus B, R = AB \oplus C, S = BD \oplus B (A \oplus D))$$

Where I_v and Q_v are input and output vectors. The symbol of IG is shown in Fig. 4. IG gate is parity preserving and also universal in the sense that it can be used for implementing parity preserving reversible full adder as shown in Fig. 5 [6-7].



Fig 4. 4*4 parity preserving reversible IG gate



Fig 5. parity preserving reversible full adder circuit using two reversible 4*4 IG gates [6-7]

New Fault Tolerant gate (NFT): NFT is a 3*3 parity preserving reversible gate that can be defined as: $I_{\nu} = (A, B, C)$

$$Q_{v} = (P = A \oplus B, Q = \acute{B}C \oplus A\acute{C}, R = BC \oplus A\acute{C})$$

Where I_v and Q_v are input and output vectors respectively. This gate has a QC of 5 and is depicted in Fig. 6. The reversible NFT gate can be used for implementing arbitrary functions [4]. The implementation of NFT gate as NOT and AND functions is shown in Fig. 7. The EX-OR function also can be obtained as shown in Fig. 8. The OR function can be implemented as depicted in Fig. 9.



Fig 6. The 3*3 Reversible NFT gate



Fig 7. The Reversible NFT gate as NOT and AND



Fig 8. The Reversible NFT gate as XOR



Fig 9. The Reversible NFT gate as OR

3. Implementation of Parity Preserving Reversible ALU

ALU is an integrated circuit that performs arithmetic and logic operations on two operands, "A" and "B". While the ALU is a fundamental component of all processors, the design and function of an ALU may vary between different processor models. Several researchers have proposed reversible ALU circuits [13-15]. These designs are not parity preserve. Fig.10 depicts existing parity preserving Arithmetic Logic Unit that is designed on John Von Neumann's ALU concept. This circuit produce four AND, OR, EX-OR and ADD operations [16].



Fig 10. Existing parity preserving reversible ALU

3.1. New Nanometric Parity Preserving Reversible ALU

This section has two parts that shows the implementation of LU (Logic Unit) and AU (Arithmetic Unit) respectively. The Fig. 11 is the general design of an ALU with respect to Morris Mano's approach [17]. It illustrates the connection between two mentioned units.



Fig 11. The General design of an ALU

3.1.1. Implementation of Our Proposed Parity Preserving Reversible LU

Logic unit is consisting of gates that produce functions and one multiplexer to select them. The proposed parity preserving reversible Logic Unit circuit using FRG and F2G gates is depicted in Fig. 12. We use NFT gates to produce the needed functions (shown in Fig. 7, Fig. 8 and Fig. 9) and the FRG gates to implement a 4*1 multiplexer. As it is stated before, in reversible logic every output can be used once and neither feedback nor fan-out is allowed [18]. For this reason we used F2G gate for copying needed values in the circuit. Table.1 shows the operations of the circuit.



Fig 12. Our proposed parity preserving reversible Logic Unit

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Table 1. Operations of the Logic Unit					
S2	S1	F			
0	0	A . B			
0	1	A + B			
1	0	$A \oplus B$			
1	1	Á			

3.1.2. Implementation of our Proposed Parity Preserving Reversible AU

Our proposed reversible Arithmetic Unit circuit is depicted in Fig. 13. In this implementation we used a parity preserving reversible Full Adder (shown in Fig. 5) and one 4*1 multiplexer using three FRG gates as shown in Fig. 12. We show the operations of circuit as a result of changing the selectors in the form of the table in Table. 2.



Fig 13. Our proposed Nanometric reversible Arithmetic Unit circuit

Table 2. operations of the Arithmetic Unit					
S2	S1	F			
0	0	A + B			
0	1	A - B			
1	0	А			
1	1	A + 1			

4. Evaluation of our Proposed Parity Preserving Reversible ALU

The proposed parity preserving reversible ALU has more operations than the existing one. Thus it is more efficient in speed of performing computations and functions. Table. 3 compares our proposed parity preserving reversible ALU with the existing design in the case of operations. In the next step, the aim is to distinguish the major parameters of the circuit.

Table 3. Comparison of the different Nanometric parity preserving reversible ALU circuits operations:									
Operations	AND	OR	EX- OR	NOT	ADD	SUB	INC	Direct transmission	Total number of operations
Existing circuit	\checkmark	\checkmark	\checkmark		\checkmark				4
proposed circuit	\checkmark		\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	8

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One of the main parameters in designing reversible circuits which can be discussed is logical calculation and is related to hardware complexity. Let

 α = A two input EX-OR gate calculation

 β = A two input AND gate calculation

d= A NOT calculation

T= Total logical calculation

Total logical calculation is the count of the XOR, AND, NOT logic in the output expressions. For logic unit of the proposed parity preserving reversible ALU, we have three FRG, three NFT and four F2G. Thus we have total logical calculation as follows:

 $T_{LU} = 23\alpha + 24\beta + 15d$

For arithmetic unit of the proposed parity preserving reversible ALU, we have two IG, three FRG and one F2G. Thus its logical calculation is as follows:

 $T_{AII} = 16\alpha + 18\beta + 8d$

And the total logical calculation of the proposed parity preserving reversible ALU is:

 $T_{total} = 51\alpha + 54\beta + 29d$

One of the other major constraints in designing a reversible logic circuit is to reduce the number of garbage outputs. Our proposed ALU circuit produces 28 garbage outputs that are optimized completely.

Number of constant inputs is one of the other main factors in designing a reversible logic circuit. Our proposed parity preserving reversible ALU circuit requires 19 constant inputs and it's most efficient number that we could achieve. For complete information you can refer to Table. 4.

Our proposed implementation is explained for one bit but it can be expanded for n bits with parallel circuits and can be used for ALU circuits with 4 or more bits. Fig. 14 depicts the proposed parity preserving reversible ALU.

Table 4. Parameters of our proposed reversible circuit at a glance.

	No. of gates	No. of garbage outputs	No. of constant inputs	Total quantum coast	Total logical calculation
Proposed LU	10	12	10	38	23α+24β+15d
Proposed AU	6	10	6	31	16α+18β+8d
Proposed ALU	22	28	19	90	51α+54β+29d



Fig 14. Our proposed Nanometric parity preserving reversible ALU circuit

5. CONCLUSION

Arithmetic and Logic Unit and its design has outstanding role in computer systems. Reversible logic circuits have received significant attention in nanoscale computer design. In this regard nowadays, designing parity preserving reversible circuit holds its importance as well. In this paper first we proposed designs of AU and LU individually. Then we show whole ALU and the connections between two units. The proposed parity preserving reversible ALU circuit is different from that of indicated in [16] in the case of design methodology. Also the performance efficiency and speed in this approach is more reliable when it is compared to the existing counterpart. The parameters of the circuit are shown in Table 4. In this table we report the number of gates, number of garbage outputs, quantum cost, constant inputs and total logical calculation for the proposed parity preserving reversible AU. We have tried to design parity preserving reversible ALU with optimum parameters and better performance to have high speed circuits. All the designs are in the nanoscale criteria in nanotechnology. Thus the proposed designs can be used to construct more complex systems in nanotechnology.

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