J. Basic. Appl. Sci. Res., 3(2s)555-560, 2013
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ISSN 2090-4304
Journal of Basic and Applied Scientific Research
www.textroad.com

Single Miller Capacitor Feedforward Frequency Compensation on Three Stage Amplifier for Large Capacitive Load

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Received: June 10 2013
Accepted: July 10 2013

ABSTRACT

This paper presents the analysis of single Miller capacitor feedforward compensation scheme which is used in three-stage CMOS operational amplifiers. single Miller compensation capacitor in three-stage amplifiers can significantly reduce the total capacitor value, and therefore, the overall area of the amplifiers without influencing their stability. Feedforward technique is effectively combined to achieve better small-signal and large-signal performances. The structure proposed in this paper compared to all previous structures, significantly higher bandwidth and phase margin. The value of the compensation capacitor is also reduces significantly. conducted Simulations in this paper was on 0.25µm for (25-kΩ//120Pf) large load.

KEYWORDS: frequency compensation, feedforward technique, three stage amplifier, single miller compensation.

1. INTRODUCTION

Design and optimization of multi-stage operational amplifiers (opamps) is becoming increasingly challengeable in modern IC technologies. While submicron transistors benefit from very high transient frequency, their low intrinsic gain significantly affects the linearity and the accuracy of analog circuits. The decrease in intrinsic gain is directly proportional to the scaling rate. Hence, to compensate for the effect of scaling on the accuracy of opamps, DC gain of each stage should be increased. As the upper limit of voltage supply is continuing to decrease in each coming technology, this is no longer possible. Another solution, compatible with low-voltage environment, is to add more cascaded stages [1-9]. Frequency compensation is mandatory to stabilize a closed-loop three-stage opamp. Among the techniques introduced for driving of large capacitive loads in three stage amplifier, Single Miller capacitor Compensation amplifier (SMC), has more advantages due to using one compensation capacitor instead of two. To achieve higher bandwidth and greater stability of a feedforward path is used. The single Miller capacitor feedforward frequency compensation amplifier (SMFFC) uses a feedforward path to provide an LHP zero to compensate the first nondominant pole. So, the bandwidth is increased. In this paper, the design was based on achieving a wide bandwidth in a high phase margin and the compensation capacitor value is reduced as much as possible. Achieving to this target, firstly review single Miller capacitor compensation amplifier (SMC). Finally, bring the result of Simulation. As will be shown in the simulations, The structure proposed in this paper has high bandwidth and stability.

2. Single Miller Capacitor Compensation Amplifier (SMC)

In most three stage amplifier structures were used two compensation capacitor to driving a large capacitor loads. But the Compensation presented in this section, only a small capacitors used for three stage amplifiers. In amplifiers with a large capacitive load, last stage poles are usually very small and it is so near to the dominant pole which is located on the first stage, and should be lower it's effect by One of the most common compensation. In Usual pole spliting has been used. In figure (1) you can see the structure of SMC amplifier.

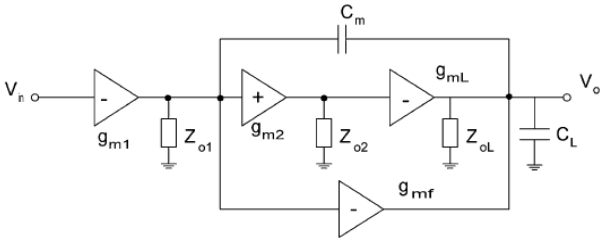

Figure1: *Topology of single Miller capacitor compensation amplifier (SMC)*

A larger bandwidth can be obtained by using only one capacitor for compensation instead of two. The structure

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has three gain stages with only one compensation capacitor. It has an additional transconductance stage (gmf) from the output of the first stage to the final output. This forms a push-pull stage at the output that helps in improving the transient response of the amplifier. A single Miller compensation capacitor (c_m) is used to split the first pole(p_1) and the third pole (p_3). The position of the second nondominant pole(p_2) is dictated by the gain of the second stage, which decides the stability of the amplifier[10].

The transfer function is given by (1):

(1)

$$AV_{(SMC)} = \frac{VO(s)}{Vin(s)} = \frac{Adc(1+s\frac{C_{p2}g_{mf}-C_m g_{o2}}{g_{m2}g_{mL}} - s^2\frac{C_m C_{p2}}{g_{m2}g_{mL}})}{(1+\frac{s}{p_{-3dB}})(1+s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}})}$$

$$\approx \frac{(1+s\frac{C_{p2}g_{mf}-C_m g_{o2}}{g_{m2}g_{mL}} - s^2\frac{C_m C_{p2}}{g_{m2}g_{mL}})}{\frac{s}{GBW}(1+s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}})}$$

Where $AV_{(SMC)}(0) = A_{dc} = (g_{m1}g_{m2}g_{mL} / g_{o1}g_{o2}g_L)$ is the dc gain of the amplifier, and $P_{3-dB} = (g_{o1}g_{o2}g_L / g_{m2}g_{mL}C_m)$ is the dominant pole of the amplifier. Hence, the gain-bandwidth product is given by $GBW = A_{dc} \cdot p_{3-dB} = g_{m1} / C_m$. From the transfer function, the amplifier has two nondominant poles and two zeros. Since the zeros are located at a higher frequency, they are neglected. The closed-loop transfer function is:

(2)

$$A_{cl(SMC)} \cong \frac{1}{1+(\frac{sC_m}{g_{m1}})(1+s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{P2}C_L}{g_{m2}g_{mL}})}$$

For large capacitive loads, the stability analysis of the amplifier can be done using the separate pole approach Assuming that the zeros of the amplifier are located at higher frequencies and hence can be neglected, the nondominant poles of the amplifier are calculated as follows.

$$P_2 = (G_{meff} / C_L) \quad (3)$$

$$P_3 = (g_{o2} / C_{p2}) \_ (G_{meff} / C_L) \quad (4)$$

$$G_{meff} = (g_{m2}g_{mL} / g_{o2}) \quad (5)$$

The value of the compensation capacitor become $C_m = \frac{1}{A_{V2}}(2\frac{g_{m1}}{g_{mL}}C_L)$. This represents a compensation capacitor is very small thus,it can be seen that by suitable choice of the second-stage gain ; $A_{v2} = (g_{m2} / g_{o2})$ ، The value of the compensation capacitor can be reduced. Note that, Zeros of the transfer function depends on the compensation capacitor if the value of this capacitor is too small, zeros are placed at very high frequencies[10].

3. Single Miller Capacitor Feedforward Frequency Compensation Amplifier (SMFFC)

Although the first nondominant pole in SMC is designed to be at a relatively higher frequency, it still influences the frequency response to some extent. This prevents the further increase in GBW and reduction in the compensation capacitor size. The proposed SMFFC, shown in Fig. 2, uses a feedforward path to provide an LHP zero to compensate the first nondominant pole. The feedforward path also adds current at the second-stage output, which increases the output conductance of the stage and pushes the pole at the output of the second stage to higher frequencies. The LHP

zero is placed near the first nondominant pole which provides a positive phase shift that compensates for the negative phase shift due to the nondominant poles[10].

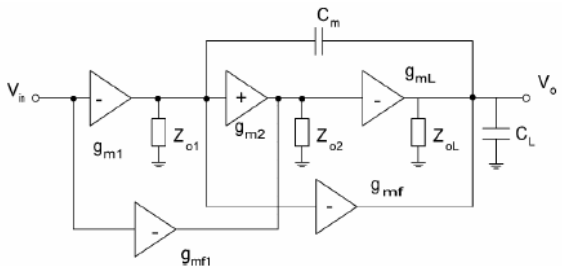

Figure2: *Topology of single Miller capacitor feedforward frequency compensation amplifier (SMFFC)*

3.1.Small-Signal Analysis

Small-signal analysis is carriedout with the following assumptions.

1. The gain of all stages are much greater than 1.
2. The Parasitic capacitances C_{P1} ,C_{P2} and C_{PL} are much smaller than the Miller capacitor C_m and load capacitor C_L
3. The transconductance of the feedforward stage, g_{mf}, is equal to that of the third gain stage, g_{mL}.

Solving the small-signal circuit model transfer function is given by

(6)

$$A_{V\,(SMFFC)(S)} = \frac{V_{O(S)}}{Vi_{n(S)}} = \frac{A_{dc}\left(1+s\frac{C_m g_{mf1}}{g_{m1}g_{m2}} - s^2\frac{C_m C_{p2}}{g_{m2}g_{mL}}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+S\frac{C_L g_{o2}}{g_{m2}g_{mL}} + S^2\frac{C_{P2}C_L}{g_{m2}g_{mL}}\right)}$$

Where $A_{dc} = (g_{m1}g_{m2}g_{mL} / g_{o1}g_{o2}g_L)$ is the dc gain of the amplifier and $p_{3-dB} = (g_{o1}g_{o2}g_L / g_{m2}g_{mL}C_m)$ is the dominant pole of the amplifier. Hence, the gain-bandwidth product is given by $GBW = (g_{m1}/C_m)$**.** For a large capacitive load, the stability analysis of the amplifier is done using the separate pole approach**.** Since the term in the numerator of (6) is negative and the term is positive, this implies that there is an LHP zero and a RHP zero. The LHP zero occurs at a lower frequency than the RHP zero. This helps to improve the frequency response**.** The non-dominant pole is obtained from the following relations:

$$P_2 = (G_{meff} / C_L) \tag{7}$$

$$P_3 = (g_{o2} / C_{p2}) \_ (G_{meff} / C_L) \tag{8}$$

$$G_{meff} = (g_{m2}g_{mL} / g_{o2}) \tag{9}$$

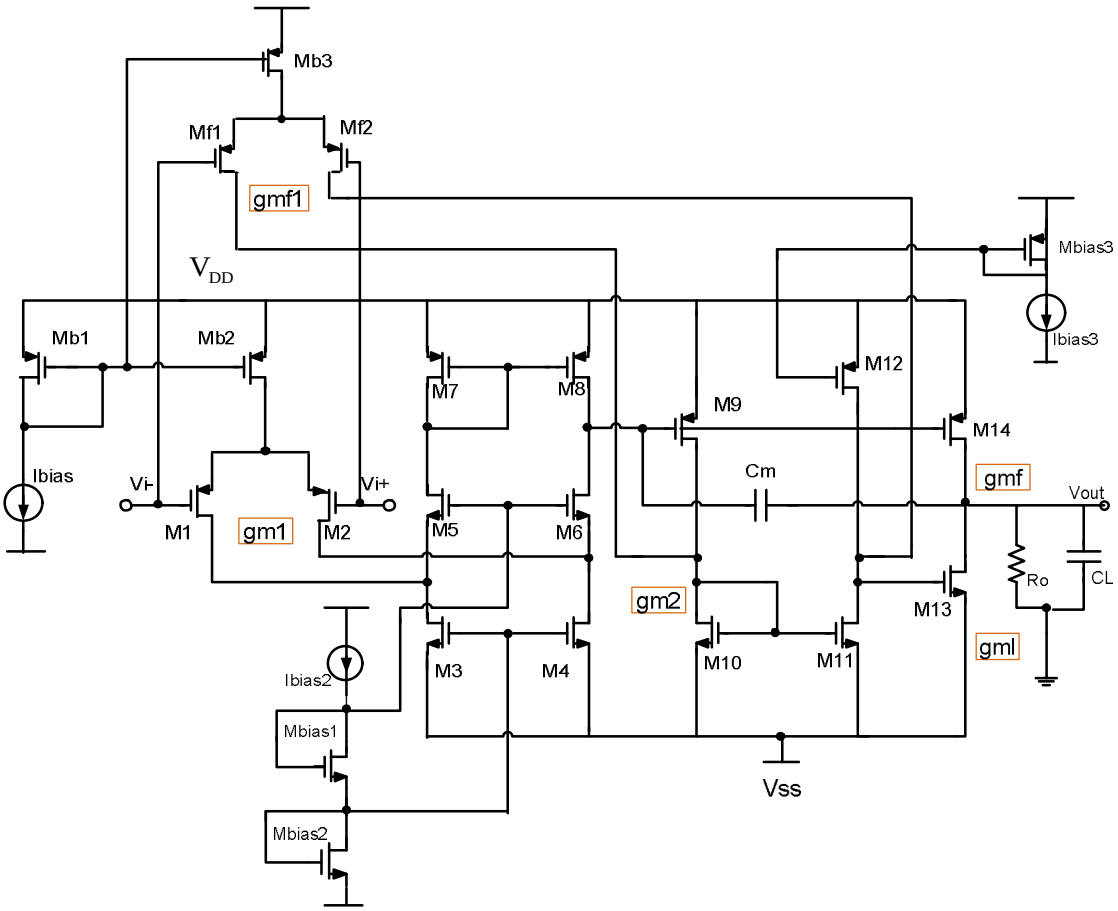

***Figure3**: Schematic of the SMFFC amplifier.*

Since the zero-pole doublet occurs at high frequency (around twice the bandwidth), the performance of the amplifier is not significantly disturbed.

3.2.Slew Rate and Settling Time

The transient response of the amplifier is comprised of the slewing and settling behavior of the amplifier in closed-loop condition. The slew rate of the amplifier depends on the size of the compensation capacitor. The significant increase in the slew rate of SMFFC as compared to that of Previous scheme under the same conditions is due to the reduction in the size of the compensation capacitor. Due to the high bandwidth of the SMFFC amplifier, this structure have a better settling time.

3.3. Design Considerations and Circuit Implementation

A judicious distribution of gain among the three stages is one of the most important considerations in the design of these amplifiers $>100dB$, the gain is distributed such that A_{v1} $A_{v2} > A_{v3}$. This results in the second and third pole of the amplifier being located at higher frequencies due to the high output conductance of the second and third stages. This roughly results in a single-pole system. In order to achieve this, the first stage uses a folded cascode topology to enhance the output impedance. A moderate gain at the second stage helps in reducing the required compensation capacitor to a great extent. The circuit implementations of the SMFFC amplifier is shown in Figs (3). transistors M_1-M_8 form the first gain stage. Transistors M_{f1} and M_{f2} form the feedforward transconductance stage ,g_{mf1}, in the SMFFC amplifier. The second gain stage of the amplifier is comprised of transistors M_9-M_{12}. The output stage is comprised of a feedforward Stage g_{mf} and the third gain stage g_{ml} forming a push-pull stage. The third gain stage is realized by transistor $M13$, whereas the feedforward stage is realized by transistor $M14$. The gate–drain capacitance of transistor M13 forms an additional Miller capacitor between the second and third stages. Since the parasitic capacitor value and the gain of the third stage are small, it is neglected.

4 . SIMULATION RESULTS

Circuit-level simulation results are obtained with 0.25 μm BSIM3 2.5 V models using HSPICE. All the results above are with a 25kΩ //120-pF load. In this paper an attempt has been done to design compensation capacitor as small as possible. capacitor is 2pf. Table (1) contains the proposed dimension of transistors which Simulations have been performed based on them. In SMFFC our target was reaching to High phase margin in a wide bandwidth. in addition, they should have High DC gain, and finally we reach to 79º phase margin in a 11.7MHZ bandwidth, which is optimum and comparing to previous models is much more better. In figure (4) you can see, Simulation of frequency response of SMFFC open loop amplifier. Among The parameters of closed loop we can mentioned settling time slew rate. Both of them are Important parameters for operational amplifiers and achieved from Transient closed-loop system status. Since this design have higher bandwidth, it have higher speed and better settling time and slew rate comparing to pervious structure. In figure (5) you can see closed-loop simulation of designed structures. with the 1.5-V step input, there is an overshoot for the up-going signal. For the low voltage and the high voltage, the operating points of the transistors in the circuit are different, which means that the effective pole, zero locations of the amplifier are different for rising and falling signals. This is the reason why overshoot appears for up-going signal, and not for down-going signal. The 0.1% settling time is considered. in table (2), a comparison between new designed and previous models has been done, then we could prove the superiority of above design.

5 . Conclusion

In this paper, single Miller capacitor feedforward compensation was presented on three stages amplifiers, and comparing to previous structures have better bandwidth and phase margin. With only a small compensation

capacitor, the area of the amplifier is reduced significantly the gain-bandwidth product is improved, and the stability condition is established. A feedforward path is added to the SMFFC amplifier to further improve the GBW and to reduce the area. In addition, compensation capacitor value is decreased significantly. Regarding to settling time and slew rate of this system have appropriate Values.

***Table 1**: Transistor Sizes*

TRANSISTOR	SMFFC
Mb1	2*(1.9/0.5)
Mb2	8*(1.9/0.5)
M1,2	8*(2.8/0.3)
M3,4	6*(0.9/0.5)
M5,6	2*(0.9/0.5)
M7,8	6*(2.8/0.965)
M9	6*(3.28/0.3)
M10,11	2*(2.5/0.48)
M12	6*(1.9/0.3)
M13	2*(8/0.32)
M14	10*(3/0.2)
MF1,2	6*(1.9/0.48)
Mb3	6*(1.9/0.5)

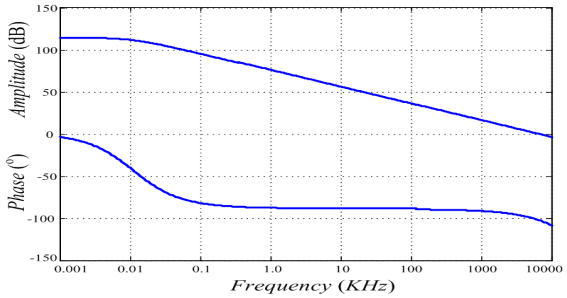

***Figure4**: opamp loop-gain frequency response of SMFFC*

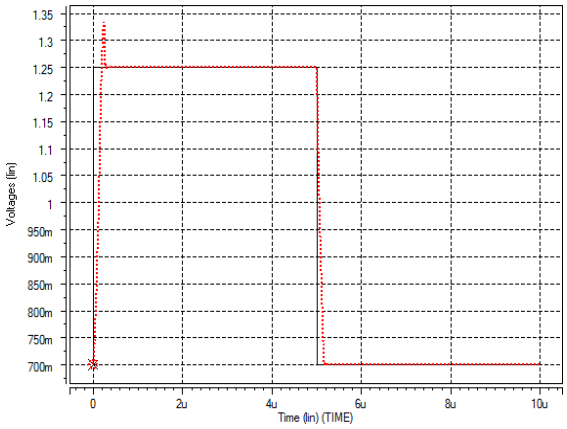

Figure5: *opamp close- loop frequency response of SMFFC*

Table2: *A comparison between multi-stage amplifiers with large capacitive load.*

PARAMETER	NMC	DFCFC	AFFC	DLPC	SMC	SMFFC	SMFFC THIS WORK
Load PF/kΩ	120/25	120/25	120/25	120/25	120/25	120/25	120/25
DC gain(dB)	>100	>100	>100	>100	>100	>100	>100
GBW(MHZ)	0.4	2.6	4.5	7	4.6	9	11.7
Phase margin	61	43	65	46	58	57	78.5
Capacitor Value (pF)	C_{m1}=88 C_{m2}=11	$_{m1}$= 18 C_{m2}=3	C_{m1}=3 C_{m2}=7	C_{m1}=4.8 C_{m2}=2.5	C_m=7 one	C_m=4 one	C_m=2 one
SR+(V/µS) SR-(V/ µS)	0.15 0.13	1.32 1.27	0.78 2.20	2.2 4.4	3.28 1.31	4.8 2	2.32 3.57
+1% TS(µS) -1%TS(µS)	4.9 4.7	0.96 1.37	0.42 0.85	0.315 0.68	0.53 0.4	0.58 0.43	0.382 0.255
Technology	0.8 µm CMOS	0.8 µm CMOS	0.8 µm CMOS	0.6 µm CMOS	0.5 µm CMOS	0. 5 µm CMOS	0.25 µm CMOS

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