J. Basic. Appl. Sci. Res., 3(2)603-608, 2013

ISSN 2090-4304
Journal of Basic and Applied Scientific Research
www.textroad.com

Survey the Inverse Property of Quantum Gates for Concurrent Error Detection

Bahram Dehghan

Department of Electrical Engineering, Sarvestan Branch, Islamic Azad University, Sarvestan, Iran

ABSTRACT

Reversible logic gates are extensively known to be compatible with future computing technologies which approximately dissipate zero heat. Concurrent Error Detection (CED) is very noticeable and widely utilized to enhance system dependability. All the inputs can be reproduced at the outputs, by utilizing the inverse property of reversible logic. Hence, by comparing the original inputs with the reproduced inputs, the errors in reversible circuits can be detected. The focus of this paper is on introducing inverse property of reversible logic gates. Also, some well-known reversible logic gates with their inverse characteristics are described. Results have been confirmed by the truth table. Finally, the proposed structures significantly show the sample circuits design for Concurrent Error Detection.
KEYWORDS: Concurrent Error Detection, Inverse property, Reversible gates

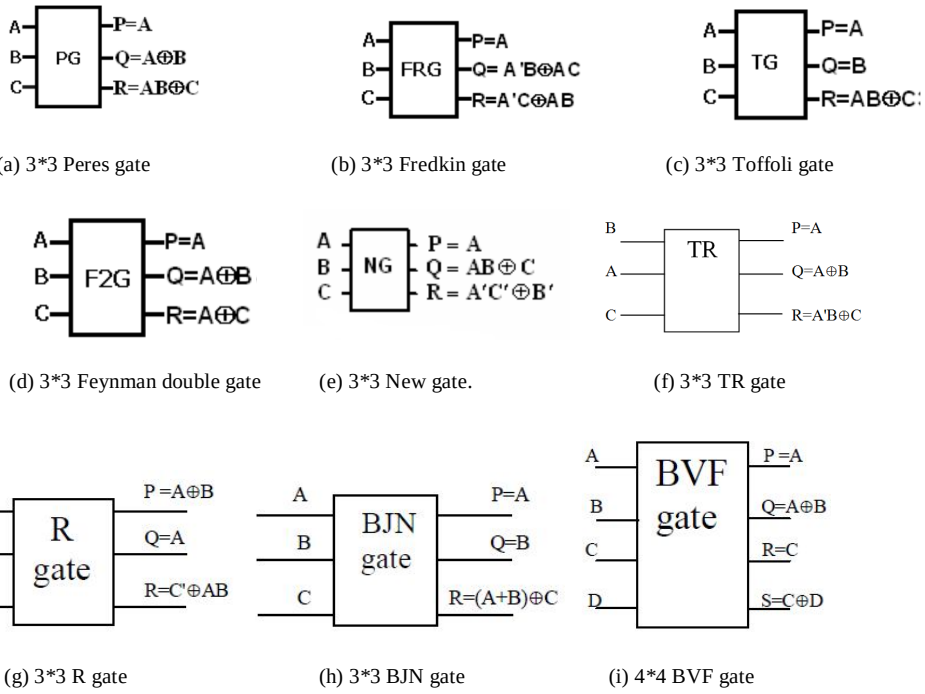
INTRODUCTION

Quantum computers are one of the most noticeable applications of reversible logic. Reversible logic is emerging as a significant research scene. Reversible circuits have applications in low power CMOS, quantum computing, digital signal processing, nanotechnology, optical computing, DNA technology and cryptography. Traditional technologies more and more start to suffer from the increasing miniaturization and the exponential growth of the number of transistors in integrated circuits. The reversible logic generates such an alternative that may replace or at least enhance conventional computer chips[1]. Specifically, a reversible logic gate must have the same number of inputs and outputs. Quantum technology is reversible and is one of the most computing technologies for future computing systems [2].To simplify the discussion, Reversible circuits are those circuits that do not lose data. Bennett [3] showed that a zero power dissipation in logic circuits is possible only if a circuit is composed of reversible logic gates [3]. The primary purpose in reversible logic design and synthesis is to minimize the quantum cost, delay and the garbage outputs. In this paper, I present a survey of some of the reversible logic synthesis that have been proposed. However, the design of inverse quantum circuits has not been adequately attended in recent literature, but I investigated some of them. Also, this paper reviews an efficient concurrent error detection scheme for inverse property of quantum gates.

REVERSIBLE LOGIC GATES

Usually it is assumed that a reversible gate has the same number of inputs and outputs. Then the output rows of the truth table of a reversible gate can be obtained by permutation of the input rows. Each output function is equal to 1 for exactly half its input assignments[4]. There exist many reversible gates in the literature. Among them, 3*3 Peres gate (PG), depicted in Fig. 1a, 3*3 Fredkin gate (FRG)[5], depicted in Fig. 1b , 3*3 Toffoli gate(TG), depicted in Fig. 1c, 3*3 Feynman Double gate(F2G) in Fig.1d , 3*3 New gate in Fig.1e , 3*3 TR gate infig.1f, 3*3 R gate in fig.1.g, 3*3 BJN gate in fig.1.h and 4*4 BVF gate infig.1.i have been studied extensively. Because of their simplicity and quantum realization cost there are design approaches and tools that incorporate them separately or in combination with each other. The truth table of these gates has not been shown because these are axiomatic.

***Corresponding Author:** Bahram Dehghan, Department of Electrical Engineering, Sarvestan Branch, Islamic Azad University, Sarvestan, Iran. Email: Bahramdehghan1@gmail.com



(a) 3*3 Peres gate (b) 3*3 Fredkin gate (c) 3*3 Toffoli gate

(d) 3*3 Feynman double gate (e) 3*3 New gate. (f) 3*3 TR gate

(g) 3*3 R gate (h) 3*3 BJN gate (i) 4*4 BVF gate

Figure 1. Some well-known reversible logic gates

CONCURRENT ERROR DETECTION

The continuous increase in the complexity of current designs generates logic circuits that are less immune to soft errors. As the soft error rate increases, Concurrent Error Detection (CED) techniques are becoming ever more essential. Concurrent error detection (CED) techniques are widely used to ensure data integrity in digital systems. Data integrity guarantees that the system outputs are either correct or an error is indicated when incorrect outputs are produced. A CED scheme based on diverse duplication compares the outputs of two different implementations of the same function and indicates an error when a mismatch occurs. The architecture of a general CED scheme is shown in Fig.2. Any CED scheme is characterized by the class of failures in the presence of which the system data integrity is preserved. CED techniques have been used for both combinational and sequential logic modules[6].

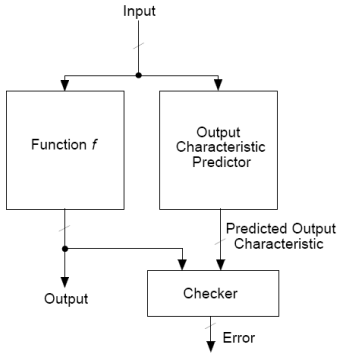


Figure.2. General architecture of a concurrent error detection scheme[6]

INVERSE AND COMPARE DESIGN OF CONCURRENT ERROR DETECTION

Concurrent error detection (CED) techniques are widely used to ensure data integrity in digital systems. Data integrity guarantees that the system outputs are either correct or an error is indicated when incorrect outputs are produced. A CED scheme based on diverse duplication compares the outputs of two different implementations of the same function and indicates an error when a mismatch occurs[6].The methodology followed in this work is

similar to the one used in[7] for reversible logic circuits. In this section, we will review the proposed technique [7]. Figure 3 shows the proposed concurrent error detection methodology. In the inverse and compare design we reproduce the inputs so errors in either monitored or inverse circuit or in both of them cannot go unnoticed. Further, since the proposed scheme results in garbage less reversible circuits it is especially suitable for reversible computing as the primary goal in reversible logic design and synthesis is to minimize the number of garbage outputs.

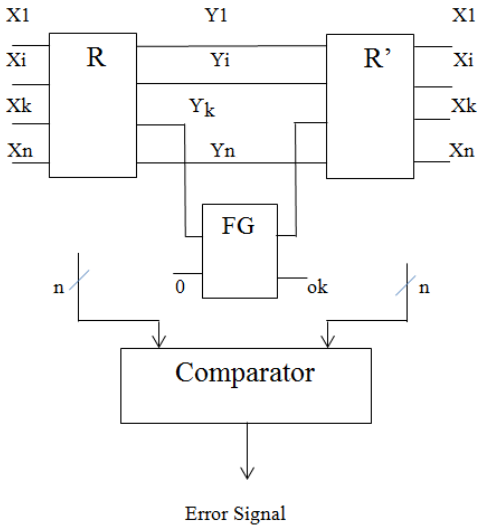


Figure.3. Proposed scheme for concurrent error detection for multi-bit errors

SURVEY THE INVERSE PROPERTY OF REVERSIBLE LOGIC GATES

In order to demonstrate the actual design of the inverse property of reversible logic gates firstly we show basic quantum gates. We called the inverse of the PG gate as the IPG gate. In order to conclude the logic equations of the IPG gate, I performed the reverse mapping of the PG gate outputs working as inputs to the IPG gate. This will reproduce the inputs of the PG gate at the outputs of the IPG gate leading to the truth table of the IPG shown in Table I. From the truth table, we can conclude the logical input and output mapping of the IPG gate shown in Fig. 4.

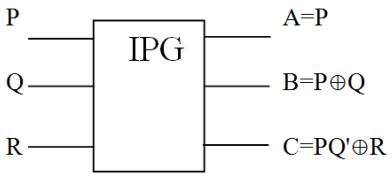


Fig.4. IPG gate

Similarly, the ITG gate is shown in fig.5. For simplification, I have utilized map method for all inverse property of quantum gates. The corresponding truth table of the ITG gate is shown in Table II.

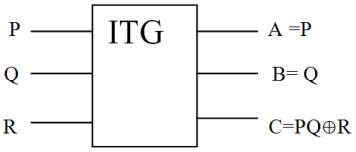


Fig.5. ITG gate

In other words, table II shows the implementation results of the described ITG gate using the inverse property.

Similarly, the IFR, IF2G, ING and IR gates are shown in fig.6, fig.7, fig.8 and fig.9 respectively. The corresponding truth table of the IFR, IF2G, ING and IR gates are shown in table III, table IV, table V and table VI respectively. The outputs are shown for every inverse property of gate.

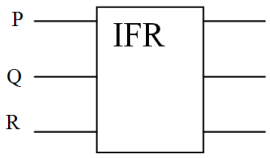


Fig.6. IFR gate

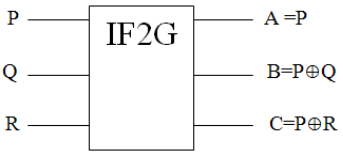


Fig.7. IF2G gate

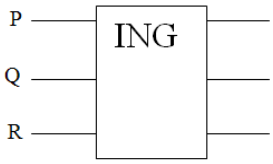


Fig8. ING gate

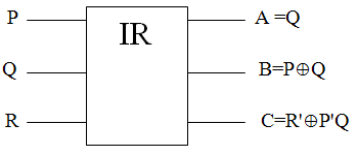


Fig.9. IR gate

Similarly, the IBJN, ITR and IBVF gates are shown in fig.10 ,fig.11 and fig.12 respectively. The corresponding truth table of the IBVF, ITR andIBJN gates are shown in tableVII, table VIII and table IX respectively.

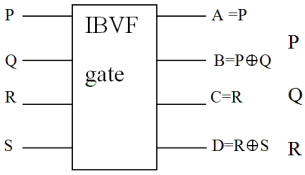


Fig.10. IBVF gate

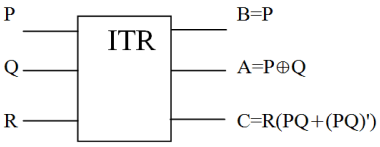


Fig.11. ITR gate

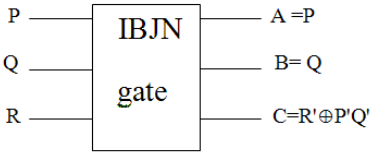


Fig.12. IBJN gate

In some cases by inversing reversible logic gates, new gates with new outputs can be achieved. Similarly, the other remain inverse reversible gates can be defined with their inputs and outputs. Also, sometimes by connecting a series of multiple gates, new gates can be achieved. For example, if two TF gates placed in series, the inputs and outputs become the same. Therefore, this structure can be used for concurrent error detection.

TABLE I. TRUTH TABLE OF IPG

P	Q	R		A	B	C
0	0	0		0	0	0
0	0	1		0	0	1
0	1	0		0	1	0
0	1	1		0	1	1
1	0	0		1	1	1
1	0	1		1	1	0
1	1	0		1	0	0
1	1	1		1	0	1

TABLE II. TRUTH TABLE OF ITG

P	Q	R		A	B	C
0	0	0		0	0	0
0	0	1		0	0	1
0	1	0		0	1	0
0	1	1		0	1	1
1	0	0		1	0	0
1	0	1		1	0	1
1	1	0		1	1	1
1	1	1		1	1	0

TABLE III. TRUTH TABLE OF IFR

P	Q	R		A	B	C
0	0	0		0	0	0
0	0	1		0	0	1
0	1	0		0	1	0
0	1	1		0	1	1
1	0	0		1	0	0
1	0	1		1	1	0
1	1	0		1	0	1
1	1	1		1	1	1

TABLE IV. TRUTH TABLE OF IF2G

P	Q	R		A	B	C
0	0	0		0	0	0
0	0	1		0	0	1
0	1	0		0	1	0
0	1	1		0	1	1
1	0	0		1	1	1
1	0	1		1	1	0
1	1	0		1	0	1
1	1	1		1	0	0

TABLE V. TRUTH TABLE OF ING

P	Q	R		A	B	C
0	0	0		0	0	0
0	0	1		0	1	0
0	1	0		0	1	1
0	1	1		0	0	1
1	0	0		1	1	1
1	0	1		1	0	0
1	1	0		1	1	0
1	1	1		1	0	1

TABLE VI. TRUTH TABLE OF IR

P	Q	R		A	B	C
0	0	0		0	0	1
0	0	1		0	0	0
0	1	0		1	1	0
0	1	1		1	1	1
1	0	0		0	1	1
1	0	1		0	1	0
1	1	0		1	0	1
1	1	1		1	0	0

TABLE VII. TRUTH TABLE OF IBVF

P	Q	R	S		A	B	C	D
0	0	0	0		0	0	0	0
0	0	0	1		0	0	0	1
0	0	1	0		0	0	1	1
0	0	1	1		0	0	1	0
0	1	0	0		0	1	0	0
0	1	0	1		0	1	0	1
0	1	1	0		0	1	1	1
0	1	1	1		0	1	1	0
1	0	0	0		1	1	0	0
1	0	0	1		1	1	0	1
1	0	1	0		1	1	1	1
1	0	1	1		1	1	1	0
1	1	0	0		1	0	0	0
1	1	0	1		1	0	0	1
1	1	1	0		1	0	1	1
1	1	1	1		1	0	1	0

TABLE VIII. TRUTH TABLE OF ITR

P	Q	R		A	B	C
0	0	0		0	0	0
0	0	1		0	0	1
0	1	0		0	1	0
0	1	1		0	1	1
1	0	0		1	1	0
1	0	1		1	1	1
1	1	0		1	0	1
1	1	1		1	0	0

TABLE IX. TRUTH TABLE OF IBJN

P	Q	R		A	B	C
0	0	0		0	0	0
0	0	1		0	0	1
0	1	0		0	1	1
0	1	1		0	1	0
1	0	0		1	0	1
1	0	1		1	0	0
1	1	0		1	1	1
1	1	1		1	1	0

Also, if four PG gates placed in series again, we have the same inputs and outputs which can be used for concurrent error detection. Figure 13 and 14 show the results.

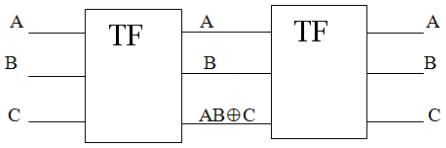


Fig13. The series of two toffoli gate

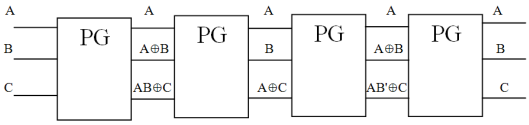


Fig14. The series of four peres gate

The currently available reversible gates can be used to implement arbitrary logic functions; however, to the best of our knowledge, the testing of such circuits has not been addressed in literature. The testing of reversible logic gates can be a problem because the levels of logic can be significantly higher than in standard logic circuits[8]. On the other hand, some gates can be used to duplicate a signal. The signal duplication function can be achieved for TR gate by setting input B to 0 as shown in Fig15.

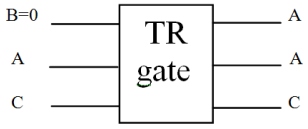


Fig15. Signal copying

Similarly, some of reversible logic gates can also be realized for signal copying. Although these circuits are simple, they are the first example of an attractive methodology for online testability. Also, several gates can be obtained same triple value at outputs. Fig 16 is shown F2G gate by setting input B and C to 0.

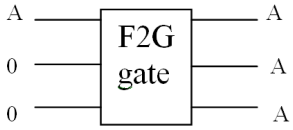


Fig16. Signal copying

Result is shown for BVF gate in fig17.a. Also, OTG gate [8] operates as a signal copying that shown in fig 17.b. Although only two outputs are equal.

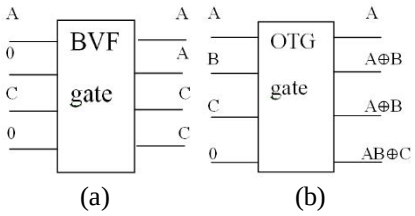


Fig17. Signal copying

The basic objective of using concurrent error detection is to perform on-line checks on the system outputs in order to guarantee data integrity by detecting temporary or permanent failures while the system is in operation[6]. By using R gate we can generate a half-adder. Figure 18 show that the R, IR and two Feynman gates from the building block of half-adder are used for concurrent error detection.

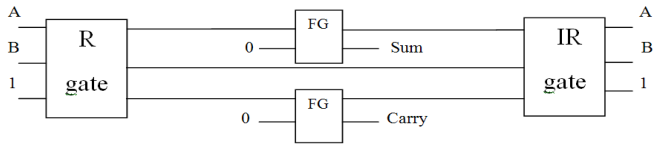


Fig18. Proposed concurrently error detection reversible half adder

Furthermore, by using TR we can produce a half- subtractor. Figure 19 show that the TR, ITR and two Feynman gates from the building block of half- subtractor are used for concurrent error detection.

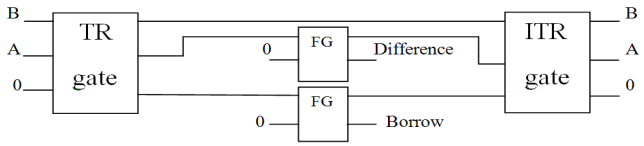


Fig19. Proposed concurrently error detection reversible half subtractor

In some cases we can use inverse property of these gates in the first building block. As a result, Concurrent Error Detection can be repeated in the following circuit by using PG and IPG gates for generating half subtractor. This architecture was proposed as indicated in Figure 20.

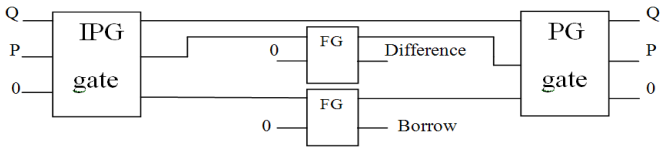


Fig20. Proposed concurrently error detection reversible half subtractor

CONCLUSION

Reversible logic synthesis is not as easy as classical logic synthesis. In these paper mostly reversible gates with their Inverse Properties is considered. Reversible gates and inverse properties of them can be used for CED. Also, we have presented some series structure of quantum gates. This structure can be utilized for testing any reversible circuit. I evaluated the inverse of these gates and it is suggested that the new outputs can be introduced occasionally as new gate. This paper examines various design choices for verify faults in reversible gates using CED. The described technique can guarantee to detect errors in mentioned circuits. For the first time, most reversible logic gates and inverse property of them is considered accurately.

REFERENCES

[1] Ravish Aradhya H V, Praveen Kumar B V, Muralidhara K N, "Design of Control unit for Low Power AU Using Reversible Logic", International Conference on Communication Technology and System Design 2011.
[2] M . Nielsen and I. Chuang, "Quantum Computation and Quantum Information," Cambridge University Press, 2000.
[3] C. H. Bennett, "Logical reversibility of computation," IBM J. Res. Develop., vol. 17, no. 6, Nov. 1973, pp. 525–532.
[4] P. Kerntopf," Synthesis of Multipurpose Reversible Logic Gates", TheEuromicro Symposium on Digital System Design, IEEE 2002.
[5] X. Susan Christina and M.Sangeetha Justine, "Realization of BCDadder using Reversible Logic", International Journal of Computer Theory and Engineering, Vol.2, No.3, June, 2010.
[6] S. Mitra," Diversity Techniques for Concurrent Error Detection", Center for Reliable Computing, June 2000.
[7] H. Thapliyal and N. Ranganathan," Reversible Logic Based Concurrent Error Detection Methodology For Emerging Nanocircuits", 10th International Conference on nanotechnology Joint Symposium with Nano Korea August 2010.
[8] Dilip P. Vasudevan, Parag K. Lala, Fellow, IEEE, Jia Di, and J. Patrick Parkerson, "Reversible-Logic Design With Online Testability", IEEE Transactions on instrumentation and measurement, vol. 55, no. 2, APRIL 2006.