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Low Voltage and Low Complexity Temperature Compensated CMOS Circuit

Navid Alaie Sheini[1], NimaAhmadpoor[2]

[1]Dept. of Electrical Engineering, Shahid Chamran University, Ahvaz, Iran
[2]Dept. of Electrical Engineering, Mahshahr branch, Islamic Azad University, Mahshahr, Iran

ABSTRACT

A 0.9Volt temperature compensated circuit is designed in the standard .18µm CMOS TSMC technology. This circuit is suitable for voltage reference application and is useful for a lower and greater supply voltage and sub-micron technology of CMOS. No BJT and resistor are used in this structure and the circuit consists of just eleven transistors. Some of CMOS transistors of the proposed circuit work in weak inversion region, which lead to realization of low voltage circuit and another work in strong inversion. The circuit offers a new temperature compensation methods can be used in many sensitive analog systems. This is simulated with 0.18µm TSMC technology. The technique which implement in this circuit is producing a current depends on v_T^2 and µ. But finally by injecting this current to a sub-threshold transistor the temperature dependence is reduced significantly. It gives temperature coefficient near 2.5 $\frac{ppm}{C^\circ}$ in considerable wide temperature range from -20°C to 180ºC with power dissipation around 1.53 µwatt at 25ºC. Also the circuit is examined in 1.1Volte supply voltage that results the temperature coefficient is changed to 4.5 $\frac{ppm}{C^\circ}$

KEYWORDS: sub-threshold, voltage reference, temperature compensation, supply voltage, temperature coefficient

INTRODUCTION

Reference voltages are important stages in many types of circuits such as: mixed signal circuits, ADCs, DACs, sensors and data acquisition and voltage regulators.

In the last few decades, research has been carried out in temperature dependence correction for voltage reference circuits. Furthermore, new available techniques and technology make it feasible to achieve low voltage, low power and low complexity.

The traditional voltage references, with curvature temperature correction, were implemented by BJTs. However because of the nonlinearity of temperature dependence these voltage references don't have very good temperature coefficient independency and because of silicon bandgap voltage 1.25v, which exceeds 1-V, there aren't suitable for low voltage applications. BJT-based voltage references have several hundred PPM/ºC and aren't appropriate for accurate applications [1, 2]

Another technique that was used in voltage reference is implementing BJT with CMOS technology to reduce the process complexity [3]. But, parasitic BJT transistors because of poor match of MOS devices don't have good respect. And these band gap references because of silicon band gap voltage and input common mode voltage which is needed for internal amplifier circuit aren't low voltage, either. Some techniques have been implemented for achieving sub-1V band gap references. These techniques are resistive subdivision [4, 5], low-threshold voltage device [6], BiCMOS process [7] and DTMOST device [8]. For achieving low temperature dependence band gap voltage reference other technique were offered such as exponential temperature compensation [9], piecewise-liner curvature correction [10], which have more complexity in circuit designing.

Another technique is using MOS transistor which works in saturation or sub-threshold regions. In some circuits all MOS transistor work in saturation region and uses resistor. In better circuits in this type, temperature dependence of resistors is considered such as µ and V_T [11]. In another circuits some of MOS transistors work in saturation and others work in sub-threshold and with (or without) resistor [12, 13]. By using sub-threshold region, we can use lower supply voltage for circuits simply but temperature compensation formula will be more complex mathematically. The remaining problem in using resistor in such circuit is low temperature compensation accuracy and more complexity in design [14]. These cause appetency to only-CMOS techniques without resistor. To achieve low voltage and low power circuit, purposed using transistor in sub-threshold region [13, 15].In this work design a voltage reference circuit only with MOS transistor without resistor. Because some of transistors work in sub-

***Corresponding Author:** Navid Alaie Sheini Dept. of Electrical Engineering, Shahid Chamran University Ahvaz,Iran, number:00989163015235

threshold, the voltage supply is under 1 volt. And another advantage of the purposed circuit is involving fewer transistors than other circuits [15]. The number of transistors in this circuit is eleven MOS only and no additional component.

I. The Proposed Voltage Reference Circuit

The complete circuit of proposed voltage reference is shown in Figure1. This circuit consists of three parts: main part, bias transistors and current mirrors and output stage.

A. Main part

Main part circuit consists of M1 to M4, which two of which operate in weak-inversion and the rest operate in strong inversion. M1 and M2 are the transistors that operate in strong inversion with equation (1).

$$I_D = \frac{1}{2}\mu_P C_{OX}\frac{W}{L}(V_{SG} - |V_{thp}|)^2 \quad (1)$$

Both drain and source of M1 connected to M2 pairs. This idea will reject variation effect of V_{DS} for the transistors. M3 and M4 work in weak inversion region. The relationship between voltage and current for PMOS in weak-inversion region is given by equation (2) [5].

$$I_D = \mu_P C_{OX} V_T^{\,2}\frac{W}{L}\sqrt{\frac{q\varepsilon_{Si}N_{CH}}{2\varphi_B}}\exp\left(\frac{V_{SG} - |V_{thp}|}{nV_T}\right) \quad (2)$$

One loop that passes through gate-source connect of transistors M1-M4 can be seen. It will be discussed that this loop can produce a current respect to $\mu_p V_T^2$.

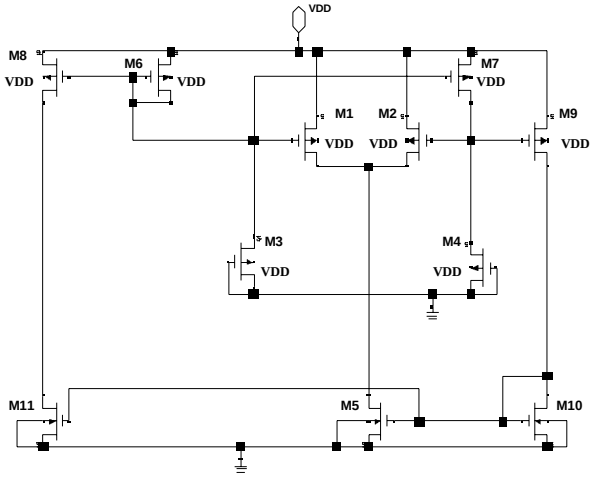

Figure 1. Circuit schematic of the proposed voltage reference

B. Bias and Current Mirror

M6 and M7 are used for M3 and M4 biasing. These transistors (M6 and M7) generate same currents which are injected into M3 and M4. M8 and M9 are mirrored and have proportional current to M6 and M2. M6 current is depended to M1 current.

C. Output Stage

M8 and M9 currents are injected to M10 and M11 which are mirrored. M10 is output transistor. This transistor is diode connected and operates in weak inversion with equation (2)

II. Principle of Reduce Temperature Dependence

As it shown in Figure 1, we can write:

$$V_{GS1} + V_{GS3} = V_{DD}$$

$$V_{GS2} + V_{GS4} = V_{DD}$$

Subtraction of above equations results:

$$V_{GS1} - V_{GS2} = V_{GS4} - V_{GS3} \quad (3)$$

V_{GS1} and V_{GS2} are gate-source voltage for transistors M1 and M2 which operate in saturation region with equation(1). M3 and M4 are operating in sub-threshold region with equation (2). By superseding transistors equations in equation (3) can reach equation (4):

$$\sqrt{\frac{2Id_1}{\mu_p C_{OX}(\frac{W}{L})_1}} - \sqrt{\frac{2Id_2}{\mu_p C_{OX}(\frac{W}{L})_2}} = nV_T Ln[\frac{(W/L)_3 Id_4}{(W/L)_4 Id_3}] \quad (4)$$

But Id1 and Id2 are related together with equation (5) and (6)

$$Id_1 + Id_2 = Id_5 \quad (5)$$

$$Id_5 = \frac{(W/L)_5(W/L)_9}{(W/L)_{10}(W/L)_2} Id_2 \quad (6)$$

By elimination of Id5 in these equations can reach to equation (7):

$$Id_1 = [\frac{(W/L)_5(W/L)_9}{(W/L)_{10}(W/L)_2} - 1]Id_2 \quad (7)$$

Simply can see:

$$Id_3 = [\frac{(W/L)_6}{(W/L)_7}]Id_4 \quad (8)$$

$$Id_{10} = [\frac{(W/L)_{10}}{(W/L)_2}]Id_2 \quad (9)$$

And finally by replacement in equation (4) can reach equation (10):

$$Id_2 = \mu_p C_{OX} n^2 V_T{}^2 [\frac{Ln\frac{(W/L)_3(W/L)_7}{(W/L)_4(W/L)_6}}{\frac{\sqrt{2K_1}}{(W/L)_1} - \frac{\sqrt{2}}{(W/L)_2}}]^2 \quad (10)$$

Where K_1 is:

$$K_1 = \frac{(w/l)_5(w/l)_9}{(w/l)_{10}(w/l)_2} - 1 \quad (11)$$

Output transistor is M10 which work in sub-threshold region and it has current: Id10 which is related to Id2 by equation (9). $V_{GS_{10}}$ Is output voltage of circuit and by using previous equations can easily find it:

$$V_{REF} = V_{GS_{10}} = |V_{th_N}| + n(\ln K_2)V_T \quad (12)$$

Where K_2 is $\frac{K_3}{(W/L)_{10}\sqrt{\frac{q\varepsilon_{Si}N}{2\phi_B}}}$ and K_3 is equal to:

$$K_3 = \left[\frac{Ln\frac{(W/L)_3(W/L)_7}{(W/L)_4(W/L)_6}}{\frac{\sqrt{2K_1}}{(W/L)_1} - \frac{\sqrt{2}}{(W/L)_2}}\right]^2 \quad (13)$$

And V_{th_N} is threshold voltage of M10, n is sub threshold slope factor and V_T is thermal voltage. K_2 is a variable which is depend on aspect values of transistors. Both V_T and V_{th_N} have temperature dependence but with two opposite slope. By tuning aspect values can generate a factor for V_T which can cancel temperature dependency of V_{th_N}.

III. SIMULATION RESULT

The Hspice simulation with 0.18µ TSMC technology was used for simulation. Simulation results have been studied for two supply voltage and the temperature range was selected from -20°C to 180ºC for both of them.

In the first simulation supply voltage is VDD=.9v. The aspect values of transistors were tuned to reach the lowest temperature affect in output voltage. In this condition according to equation (10), Id_2 is related to $\mu_p V_T^2$.

Furthermore, both μ_p and V_T have temperature dependency: $\mu_p \propto T^m$ where T is temperature and 'm' is constant near $\frac{-3}{2}$ and $V_T \propto T$ as result $Id_2 \propto \mu_p V_T^2 \propto \sqrt{T}$ .Figure 2 shows the HSPIC simulation of Id_2 vs. temperature.

The simulation results show that the proposed voltage reference generates a mean reference voltage of about 406.62mv. The important MOS parameters used in this simulation is Vth(M10) which is equal to 480mv ,the simulated temperature coefficient of the voltage reference is TCR=2.46 PPM/ ^{O}C, for the extended temperature range of -20 ^{O}C <T<180 ^{O}C .Figure 3 shows the output voltage vs. temperature with VDD=.9v.

The second simulation is done by changing supply voltage to VDD=1.1v. The output voltage is shown in figure (4). The average output voltage in this condition is 476mV and the temperature coefficient in this condition was increasing to TCR=6.3 PPM/ ^{O}C for the extended temperature range of -20 ^{O}C < T <180 ^{O}C , however temperature dependency remained low. Figure 4 shows the output voltage vs. temperature with VDD=1.1v.

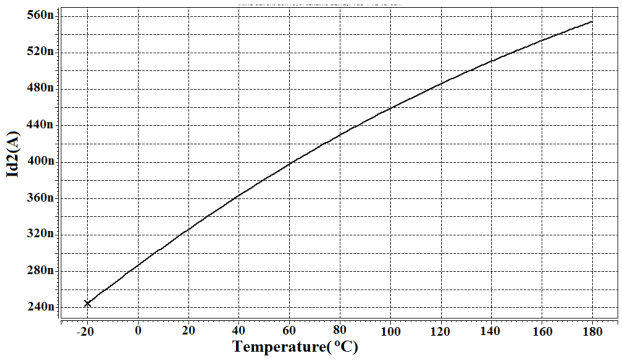

Figure 2. The M2 drain current vs. temperature (VDD=0.9v)

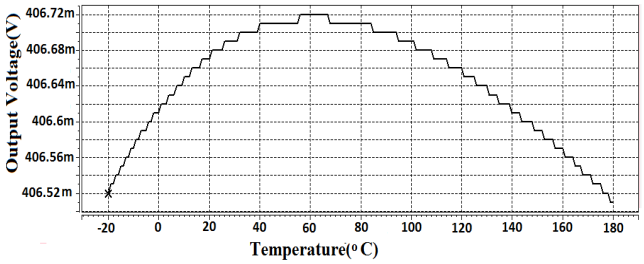

Figure 3. The output voltage vs. temperature (VDD=0.9v)

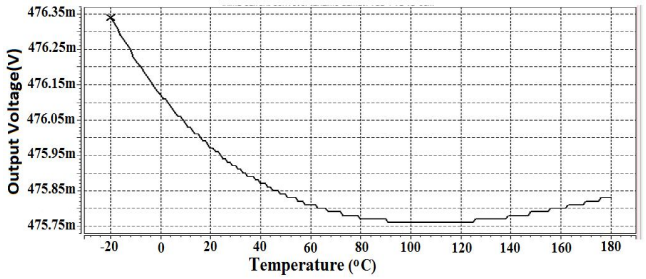

Figure 4. The output voltage vs. temperature (VDD=1.1v)

IV. Conclusion

A low voltage CMOS circuit with only eleven standard CMOS transistors and without extra element has been described for voltagereference application, which need low temperature dependency. Temperature compensation theory was studied with HSPICE simulation which illustrated very good TC, near 2.5 PPM/ºC, compared to other works and it has wide temperature range, from $-20^{\circ}C$ to $180^{\circ}C$. This circuit is low power too, with power consumption: $1.53\mu Watt$ at $25°C$ through $0.9V$ supplyvoltage. In Table 1 this work has been compared with some others. This table shows the advantages of proposed circuit especially lower TC in wider temperature range.

	Process	Temp Range(°C)	TC PPM/°C	Extra device	Minimum Supply(V)	Power (μWatt)
[13]	0.18 μm CMOS	-40 to 85	4.6	none	0.58V	0.0348 @ 0.58V
[15]	0.13 μm CMOS	-55 to 90	5	none	0.76V	0.471 @ 0.76V
[14]	0.18 μm CMOS	0 to 130	19	resistor	0.7V	119 @ 0.7V
[12]	0.6 μm CMOS	-40 to 120	37.4	resistor	1.4V	5.6 @ 1.4V
This work	**0.18 μm CMOS**	**-20 to 180**	**2.5**	**none**	**0.9V**	**1.53 @ 0.9V**

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