J. Basic. Appl. Sci. Res., 2(6)5952-5963, 2012

ISSN 2090-4304
Journal of Basic and Applied Scientific Research
www.textroad.com

A 60-µW, 98-dB SNDR and 100-dB Dynamic Range Continuous Time Delta Sigma Modulator for Biological Signal Processing in 0.18-µm CMOS

Hamid Reza Sabouhi[1], Mohammad Honarparvar[2*] and Vahid Sabouhi[3]

[1]Department of Electrical Engineering, Islamic Azad University, Jiroft Branch, Jiroft, Iran
[2,3]Department of Electrical Engineering, Sahand University of Technology, Tabriz, Iran

ABSTRACT

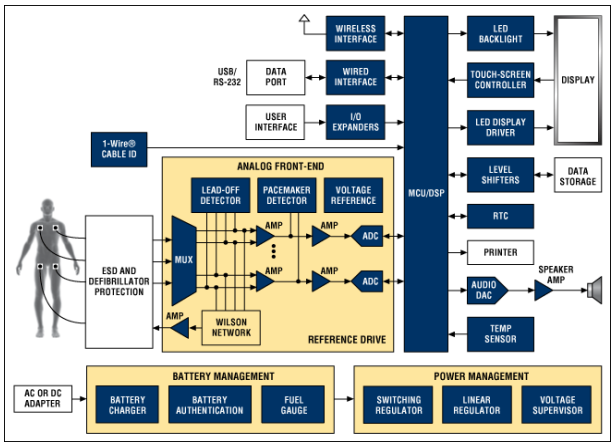
This paper presents the design of a high performance micro power modified 3rd order Continuous Time Delta Sigma Modulator intended for digitizing biomedical signals. A distributed feed forward topology is used in order to achieve efficient operation and also the modulator makes use of a Noise Shaping Enhancement (NSE) technique for increasing the performance of the modulator. g_m over I_D method is opted for design of the low power analog cells. The modulator operates on the 50 kHz signal bandwidth with sampling frequency of 3.2 MHz and shows 102 dB Signal to Noise + Distortion Ratio (SNDR) in the presence of a wide variety of circuit non-ideal effect including noise in the system level and 98 dB SNDR in the circuit level. This corresponds to an Effective Number of Bits (ENOB) 16 Bits. The modulator dissipation is 60 µw so the modulator is suitable for use in low power low cost biomedical instrument.

KEYWORDS: Delta Sigma Modulator, Micro power, Biomedical circuit, g_m over I_D.

INTRODUCTION

Demand for portable device such as wireless communication systems, battery powered medical devices, etc lead to development of the micro power circuits and analog cells. Since most physiological signals have low amplitude and low frequency the front end IC design is essentially important. These front-end ICs are used for recording the biological signals from a large number of electrodes as shown in Figure 1. According to this figure, analog to digital converter is considered as a part of Application Specific Integrated Circuit (ASIC) for digitizing the biological signals such as electrocardiogram (ECG), Electroencephalography (EEG) or Electrocardiography (ECOG) waveforms.

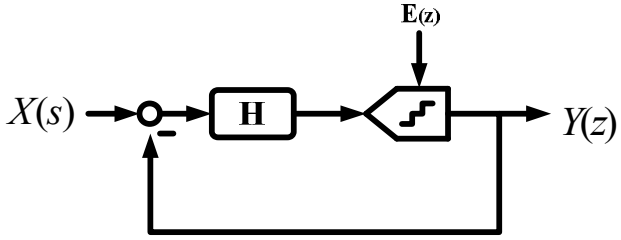
Figure 1: Analog front-end for biological signals



Among the different type of data converters, Delta Sigma modulators (DSMs) are so attractive thanks to the implicit tradeoff between resolution and bandwidth and robustness to circuit imperfections. In fact the DSMs achieve high accuracy data with low accuracy analog blocks [(1)]. The general block diagram of DSM is shown in Figure 2.

***Corresponding Author:** Mohammad Honarparvar, Department of in Electrical Engineering, Sahand University of Technology, Tabriz, Iran.

Figure 2: General block diagram of DSM



According to this block diagram if the loop filters implements in discrete time domain, the DSM is known as DT-DSM and similarly if the loop filters implements in continuous time domain the modulator is named CT-DSM. The use of CT loop filter provides several advantages over DT counterpart such as low Gain Band Width (GBW) requirement of the Operational amplifier in CT compared with DT counterpart which is suitable for low power applications. Also no Anti-Aliasing Filter (AAF) and no RC isolation circuits are required which results in further power saving [(1)].

Many different type of micro power DSM have been published in the literature. Goes et al. reported a micro power DSM in 0.18 µm CMOS. The modulator shows 80 dB SNDR over 10 kHz bandwidth with 200 µw power consumption [(2)]. Another micro power modulator with 25 kHz bandwidth by Pun et al. is designed in 0.18 µm CMOS process. It shows 74 SNDR with 300 µw power consumption [(3)]. Most recently Balagopal et al. presented a DSM with 110 µw power consumption in 0.15 µm CMOS technology. It achieves 92.4 SNDR over 6 kHz bandwidth with 110 µw power consumption [(4)]. As stated in the previous findings, decreasing the power consumption without losses the performance of the modulator is a main challenge. In this research, we are going to design a micro power (less than 100 µw) and high performance (more than 90 dB SNDR) CT-DSM.

The object of this paper is to describe the design and simulation of a micro power CT-DSM in both system and circuit level for digitizing the biological signals in the bio instruments. This paper is organized as follow: section 2 explains system level design of the CT-DSM. Section 3 discusses circuit design of the analog cells through g_m over I_D method. Simulation results are presented in section 4 and eventually conclusion are given in section 5.

2. CT-DSM System Level Design

This section is addressed system level design of the CT-DSM for biomedical applications. At first a compromise between the modulator parameters is done to select the better choices. Topology selection is considered and explained afterward and the effect of the feed forward topology for low-power design is investigated. A NSE technique is described for increasing the performance of the modulator without increasing the active analog clocks. The effect of non-idealities such as finite op-amp DC gain and finite GBW on the system is also illustrated.

2.1. Parameters Exploration

The Dynamic Range (DR) of the modulator can be calculated by the following equation [(5)]:

$$DR = f(L, OSR, B) = \frac{3}{2} \cdot \frac{2L+1}{\pi^{2L}} \cdot OSR^{2L+1} \cdot (2^B - 1)^2$$

The variables in the above equation include the resolution of the quantizer (B), the loop filter order (L) and the Over Sampling Ratio given by $\mathrm{OSR} = f_s / 2f_o$ where f_s is the sampling frequency and f_o the modulator bandwidth. According to target Signal to Noise Ratio (SNR) of more than 98 dB, the decision of the above system parameters is considered. For more power saving the OSR can be selected as low as possible. The loop filter order can be considered for the modulator stability. Finally it can be seen that modified 3rd order CT with 1 bit internal ADC is a suitable choice to achieve the better performance and low power dissipation for biomedical signals. The OSR is set to 32 for 3.2 MHz sampling frequency.

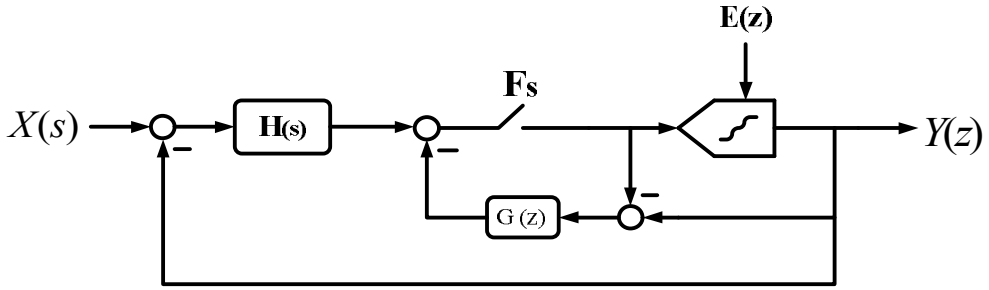
2.2. Topology Selection

In this design, a single loop low pass modulator topology is selected because of low sensitivity to circuit imperfections compared with MASH structure [(6)]. There are two single loop topology which may be used to implement the proposed CT-DSM. Feed Forward (FF) topology and Feed Back (FB) topology. The FF topology is applied in this design thanks to several reasons: lower swing requirement

for the integrators and higher power efficiency. Also the number of feedback DACs in the FF architecture is less than in the FB topology that lead to lower power dissipation [7].

As stated before, reducing the power dissipation is the major challenge in the portable biomedical instrument. To achieve the better power efficiency, reducing the number of integrators can be a solution. A Noise Shaping Enhancement (NSE) technique has been reported that yields a higher order noise shaping with less number of integrators and a successful design is done by this technique in [8]. In an abbreviated manner, we describe this method. In this technique the DSM increases the noise shaping performance from L^{th} order to L+1 th order by extraction the quantization noise and injection of quantization noise into the loop filter with one delay cycle. The NSE technique does not change the Signal Transfer Function (STF) of the modulator and the stability of the modulator preserves. Figure 3 shows the block diagram of the NSE-DSM [9].

Figure 3: Block diagram of Noise Shaping Enhancement DSM



According to Figure 3, in DT-DSM (H(s) replaced by H (z)), if the noise shaping transfer function (NTF) of conventional modulator and G (z) define by the following formulas:

$$NTF(z) = (1 - z^{-1})^{L}$$

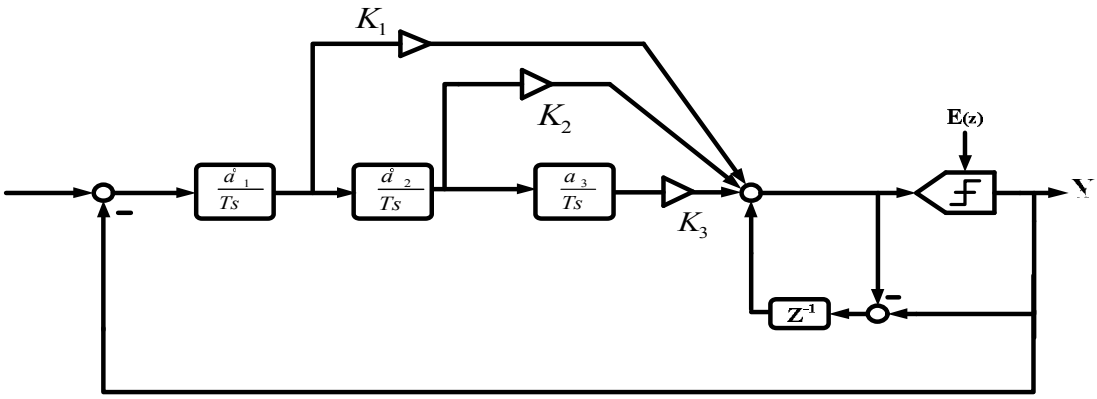
$$G_{ij}(z) = z^{-1} \sum_{k=0}^{N-1} (1 - z^{-1})^{k}$$

The Noise Transfer Function of NSE-DSM can be written as following:

$$NTF_{NSE}(z) = NTF(z)[1 - G_{ij}(z)]$$

Therefore the order of modulator will be effectively increased just by adding some passive capacitors and switches. Similar to DT-DSM, NSE technique can be applied to increase the noise shaping performance for CT-DSM. In fact if the CT and DT modulator's open loop responses from the sampled quantizer output to the sampled quantizer input are made the same then the modulator exhibit similar close loop dynamic behavior. Combined with above consideration a 3rd order CT-DSM with NSE technique is proposed in this design as shown in Figure 4.

Figure 4: Proposed modulator for micro power CT-DSM



A typical NTF of $(1\text{-}Z^{-1})^3$ is chosen for this design and coefficients of the CT-DSM is calculated as a function of the DT integrator coefficient by using the impulse invariant transform. The coefficients of the CT-DSM for None Return to Zero (NRZ) DAC pulse shaping are listed in Table 1.

2.3. Integrator Output Scaling

Saturation of the integrators is a challenge in the DSM, if the output voltage level of integrators becomes too large. To solve this problem a scaling coefficients is done for this design to serve a reasonable signal swing at each integrator output [10]. This scaling procedure can be expressed in three steps:

1. Divide ith gain of integrator by α_i (called scaling factor)

$$\alpha_i = \frac{OUT_{i-max}}{OUT_{i-desired}}$$

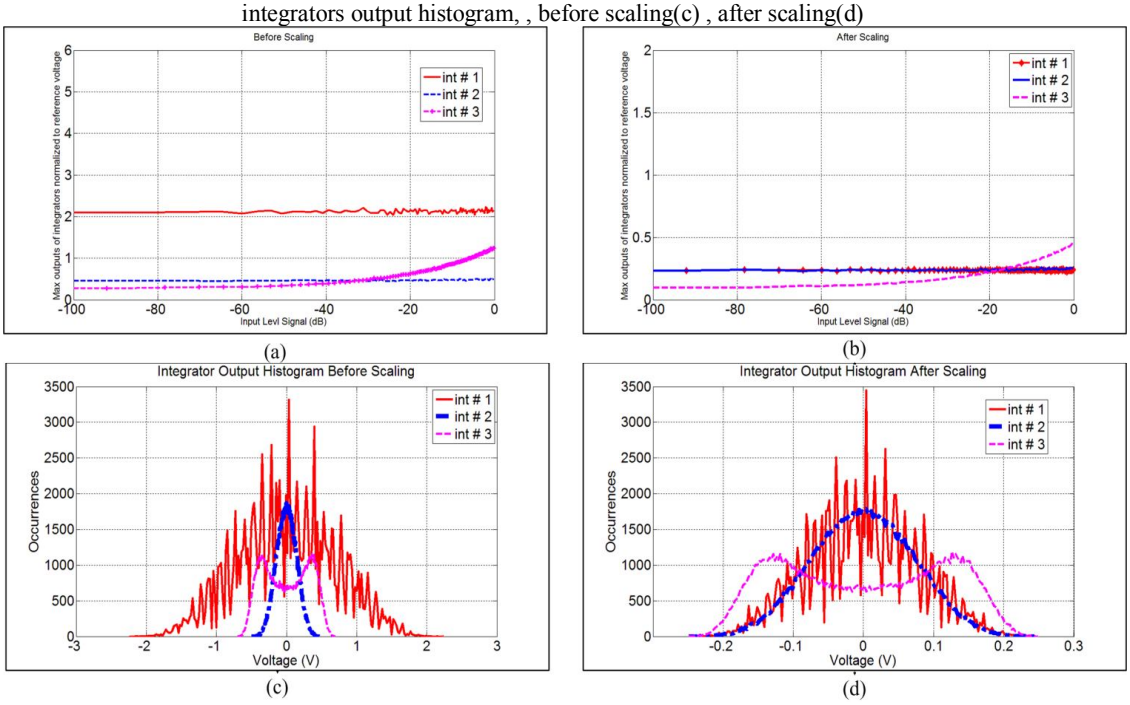
2. Distribute α_i in the modulator to preserve the same NTF
3. Perform several iterations to find the scaling factors α_i

In our design, we select the output swing of $\frac{V_{ref}}{4}$ for all integrators to achieve 16 bit resolution. Table 1 also shows the final coefficients of the modulators after scaling for the proposed design and Figure 5 illustrates the max output swing of integrators versus input signal level and the integrators output histogram before and after scaling. It can be observed from these figures that the output swing of the integrators set to 0.25 of the reference voltage and satisfy the technology requirement.

Table 1: Coefficients of the modulator before and after scaling

Coefficients	K_1	K_2	K_3	a_1	a_2	a_3	h_{DAC1}
Before Scaling	1.84	2	1	1	1	1	1
After Scaling	16.4171	3.8888	2.7952	0.1117	4.6054	0.6956	1

Figure 5: Max output swing of integrators versus input signal level , before scaling(a) , after scaling(b) - integrators output histogram, , before scaling(c) , after scaling(d)



2.4. Non Idealises Effects

A set of behavioral simulations were done in MATLAB / SIMULINK environment to optimize the performance of the modulator and extract the analog building blocks specifications. Also several non-idealities such as finite DC-gain, Gain Band Width (GBW) and sampling jitter were include investigating the effectiveness of these non- idealities on the performance of the modulator.

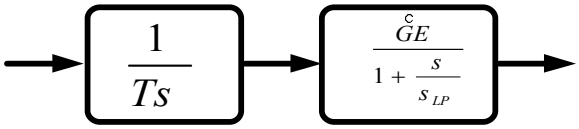
2.4.1. OTA Requirements

Usually in the CT-DSM, the CT-integrator can be implemented by active-RC integrators or Gm-C integrators, in this design we chose active-RC integrators implementation thanks to its high linearity and low noise characteristics. The ideal transfer function of the active-RC integrator can be shown as follow:

$$I(s) = \frac{1}{RCs}$$

But in real implementation, the OTAs suffer from non-idealities such as the finite DC-gain and finite GBW. Therefore the transfer function of the integrators deviates from its ideal case [11]. It can be shown that, the integrator can be modeled as a cascade of ideal integrator and first order low pas filter as illustrated in Figure 6.

Figure 6: Block diagram of real integrator

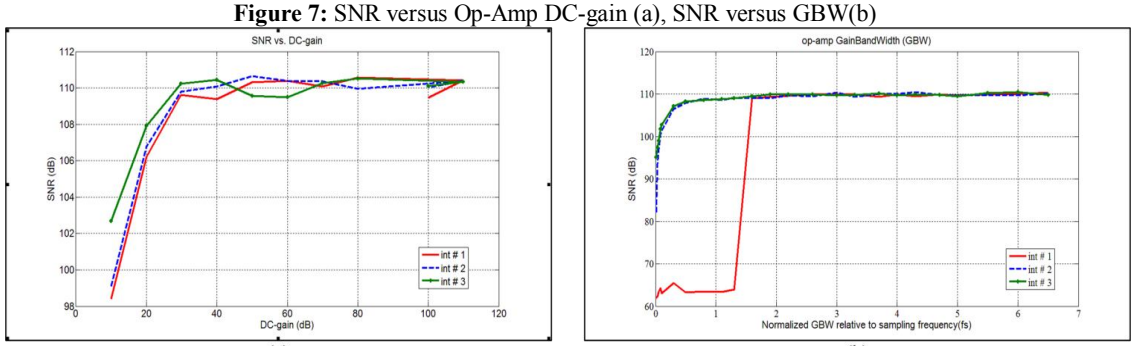


$$GE = \frac{2\pi GBW}{\frac{1}{RC} + 2\pi GBW}$$

$$S_{LP} = (\frac{1}{RC} + 2\pi GBW)$$

For the proposed design, MATLAB simulations were done to determine the DC-gain and GBW of the OTAs. Figure 7 shows the SNR versus DC-gain and GBW. According to these results a minimum DC-gain of 40dB was chosen for all OTAs and a minimum GBW of $2f_s$ was selected for the first OTA and $0.5f_s$ was selected for the second and third OTAs.

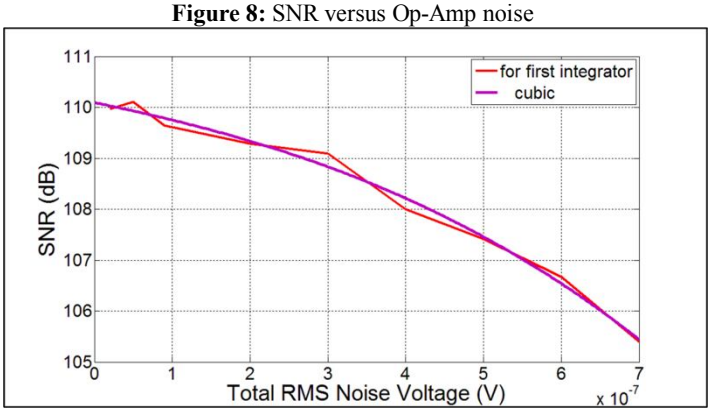
Figure 7: SNR versus Op-Amp DC-gain (a), SNR versus GBW(b)



(a) (b)

From the stand point of the noise requirement, the design of the first stage of the DSM is more critical because the noise of the first OTA is directly added to the signal without any attenuation. Op-Amp noise modeling was performed in this design similar to [12]. The total rms noise voltage includes effects from wideband thermal noise, flicker noise and DC offset. Figure 8 shows the SNR versus the total rms noise voltage.

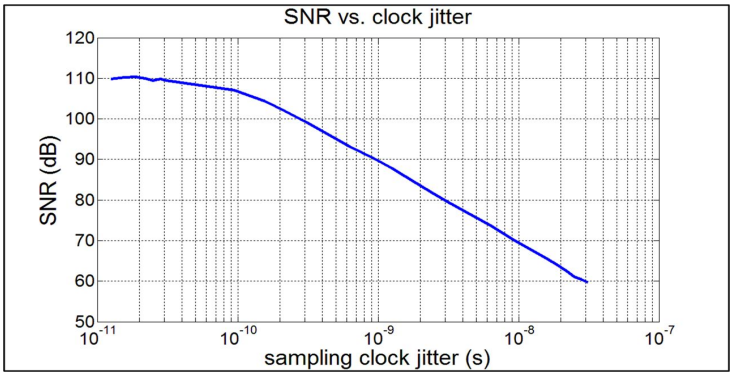
Figure 8: SNR versus Op-Amp noise



2.4.2. Sampling Jitter and Excess Loop Delay

The effects of clock jitter and excess loop delay on a CT-DSM are two major key issues. Due to low sampling frequency and negligible comparator delay, the effect of excess loop delay is not more sensitive. Commonly the noise due to the clock jitter sets a sever SNR degradation for a CT-DSM. Figure 9 shows the SNR versus the sampling jitter. In this case 7 ps sampling jitter is acceptable in order to not severely degrade the performance.

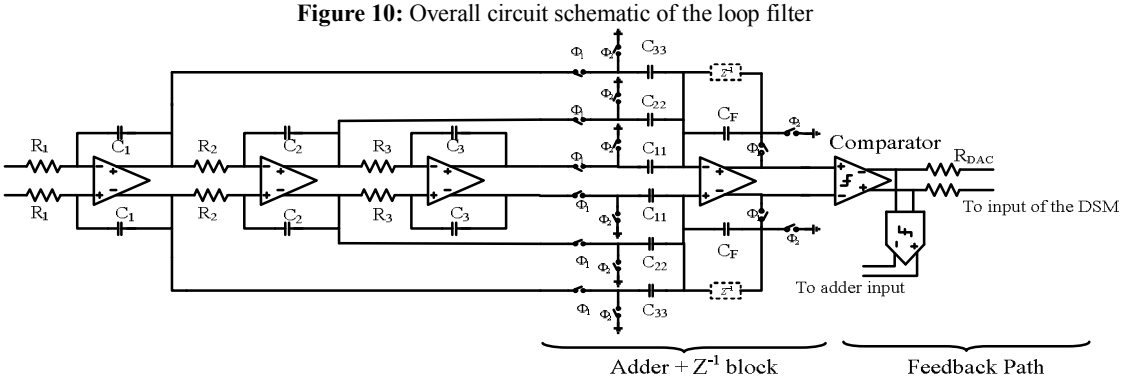
Figure 9: SNR versus sampling jitter



3. CT-DSM Circuit Level Design

The design of modulator is an iterative process between system level and circuit level. The overall circuit schematic of the modified 3rd order CT-DSM is illustrated in the Figure 10. The modulator is designed in TSMC 0.18 µm CMOS process with 1.8 V supply voltage. The implementation of each block of CT-DSM including Loop Filters, Comparator as a quantizer and active adder with SC circuitry is investigated in this section.

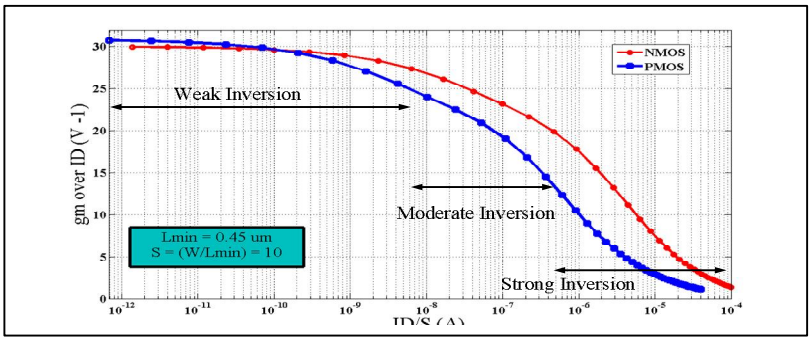
Figure 10: Overall circuit schematic of the loop filter



3.1. Loop Filter Design

As stated before the power consumption is a major challenge in the biomedical instrument. A power saving can be done by a proper design in both system and circuit level. In the system level, a NSE technique considered for low power design. But there are several techniques in the process level for designing low voltage low power circuits such as voltage boosting technique, floating gate technique, sub-threshold technique [13]. A sub threshold technique based on g_m over I_D method is opted for designing OTA used in the integrators. The design methodology based on g_m over I_D characteristic proposed by [14] allows a unified synthesize methodology in the strong inversion, moderate inversion and weak inversion. In this method a relationship between the ratios of the transconductance (g_m) over the normalized drain current ($\frac{I_D}{S}$) is considered to explore the design space as shown in Figure 11. According to this figure, when the maximum available current determined, we can achieve ($\frac{I_D}{S}$) for the corresponding ($\frac{g_m}{I_D}$). More details will present in the next subsection.

Figure 11: gm over ID versus current density



3.1.1. First Integrator Design

First integrator is known as a golden integrator. The power consumption of this integrator is the major contributor to the overall power consumption in the DSM. There is much architecture available. Some of the commonly used architectures are compared in Table 2 [15]. In order to combine the high gain and low power requirement a Telescopic OTA is selected for the first integrator. It is necessary to mention that the Telescopic OTA suffers from the limit output swing compared to Folded Cascode OTAs and Two Stage OTAs. In our design voltage scaling has been down in the system level to guarantee the output swings of the integrators are not too large.

Table 2: Commonly used architecture OTAs

Topology	Gain	Output Swing	Speed	Power Consumption
Telescopic	Medium	Medium	Highest	Lowest
Folded Cascode	Medium	Medium	High	Medium
Two Stage	High	Highest	Low	Medium
Gain Boosted	High	Medium	Medium	High

The operating modes of MOS can be separated into the following modes [14]:

1. Weak inversion mode (known as the sub-threshold)
2. Moderate inversion
3. Strong inversion

As shown in Figure 11. The features of each region are summarized in Table 3.

Table 3: Operating modes of MOSFETs

Region	Features
Weak Inversion	higher transconductance, larger g_m over I_D, smaller current, low thermal noise, low GBW applications
Strong Inversion	a compromise between the low power consumption of weak inversion and high speed of strong inversion
Moderate Inversion	smaller g_m over I_D, high GBW application

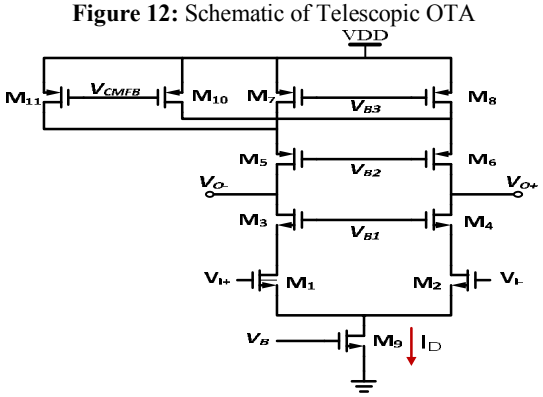
As illustrated in Figure 11 and Table 3, the weak inversion is more suitable for low power design because it provides higher g_m over I_D with smaller current.

Figure 12 shows the schematic of Telescopic OTA. According to this figure MOSFETs $M_1 - M_4$ are the core of the OTA and $M_5 - M_8$ role as load and finally M_9 provide the DC-bias current. The open loop gain and the GBW of the OTA are given by the following formulas.

$$GBW = \frac{g_{m1}}{2\pi C_L} = \frac{g_{m1}}{I_D} \cdot \frac{I_D}{2\pi C_L}$$

$$A_v = \frac{g_{m1}}{I_D} \cdot \frac{g_{m3}}{I_D} \cdot \left(\frac{1}{\lambda_n^2 + \lambda_p^2}\right)$$

Figure 12: Schematic of Telescopic OTA



Where, gm_1 and gm_3 are respectively the transconductances of transistors M_1 and M_3. I_D is the bias current flowing in MOSFETs M_1, M_2, and M_9. C_L is the capacitance at the output node, λ_N and λ_P are the parameters related to channel length modulation respectively for NMOS and PMOS devices. This OTA is designed based on the $(\frac{gm}{I_D})$ procedure reported by Silveira. The design flow of this strategy is shown in Figure 13 and the performance summary is listed in Table 4.

Figure 13: Telescopic OTA design flow graph

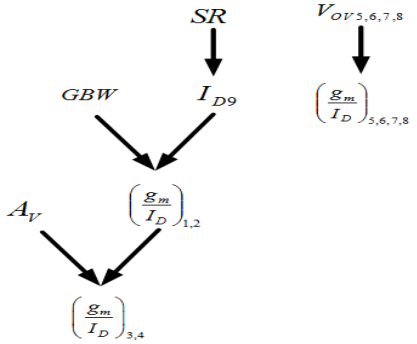


Table 4: Telescopic OTA specifications

Telescopic OTA characteristic (first stage)	value
Dc-gain	50 dB
GBW	10 MHz
Phase Margin	68°
SR	1.5V/µs
Power	20 µW

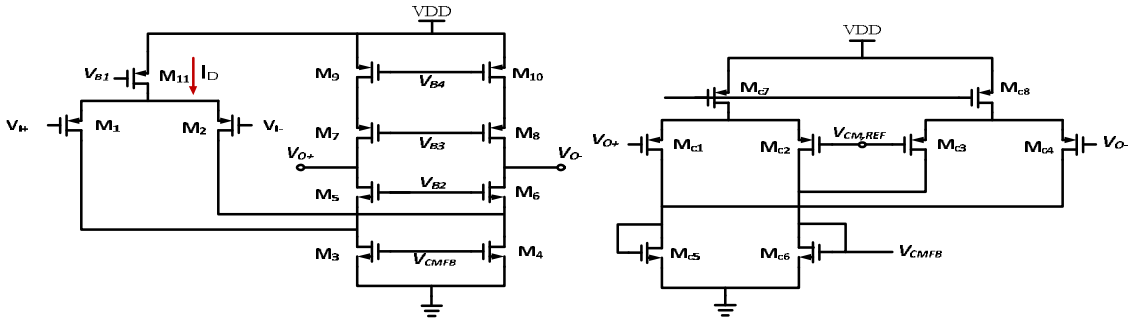
3.1.2. Second and Third Integrator Design

Since the choice of the input common mode level is easier for the folded cascode OTA, this topology is selected for second and third stages [15]. On the other hand, these stages are relatively less critical than the first stage therefore the current is scaled down to reduce power consumption. Figure 14 shows the folded cascode OTA and its CMFB. For this OTA the open loop gain and GBW are given by:

$$GBW = \frac{g_{m1}}{C_L} = \frac{g_{m1}}{I_D} \cdot \frac{I_D}{C_L}$$

$$A_V = \frac{g_{m1} \cdot g_{m6} \cdot g_{m8}}{I_D^2 (g_{m8}\lambda_n^2 + g_{m6}\lambda_p^2)} \Big|_{g_{m6}=g_{m8}} = \frac{g_{m1} \cdot g_{m6}}{I_D^2 (\lambda_n^2 + \lambda_p^2)}$$

Figure 14: Schematic of Folded Cascode OTA and CMFB



Also g_m over I_D method is applied to this topology for determining the dimensions of the MOSFETs. Figure 15 indicates the design flow of the folded cascode OTA through g_m over I_D method and Table 5 shows the specifications of the designed folded cascode OTA.

Figure 15: Folded cascode OTA design flow graph

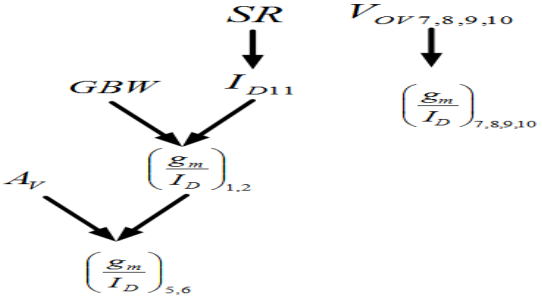


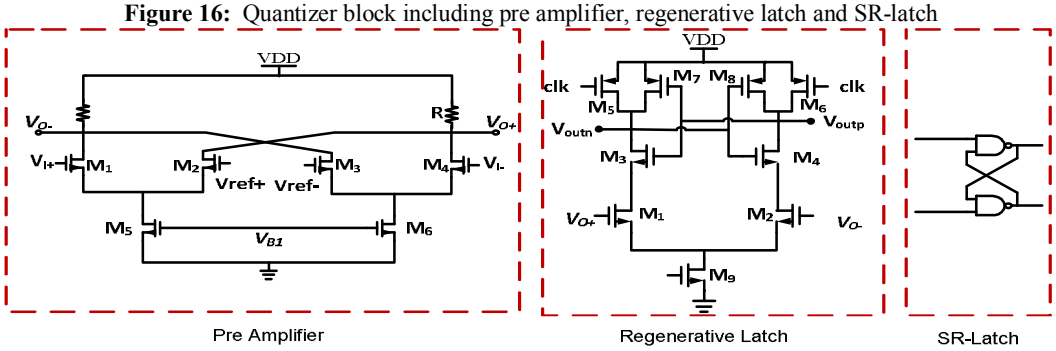
Table 5: Folded cascode OTA specifications

Folded cascode OTA characteristic (second and third stages)	value
Dc-gain	53 dB
GBW	3 MHz
Phase Margin	63°
SR	1V/µs
Power	13.5 µW

3.2. Preamplifier and Comparator Design

The schematic of the 1bit quantizer including pre amplifier, regenerative latch and SR latch used in the proposed micro power CT-DSM is shown in Figure 16. Because of decreasing the offsets and kick-back noise from the latch a Differential Difference Amplifier (DDA) with resistive loads is used for the pre amplifier. A dynamic regenerative latch is used because it is a power efficient structure [5]. The power consumption of the designed comparator is 2.9 µw at a 3.2 MHz sampling frequency.

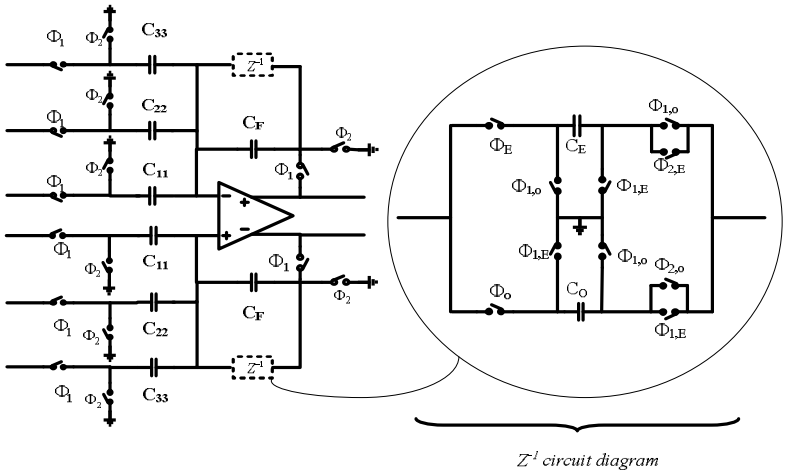
Figure 16: Quantizer block including pre amplifier, regenerative latch and SR-latch



3.3. Active Adder with SC circuitry and one cycle delay block

In the conventional FF topology, an active-R adder uses in the close loop configuration. But in this design, thanks to the Z^{-1} block, coupling of the quantization error is unpractical. To overcome this problem an active adder using SC circuitry is used as shown in Figure 17. On the other hand, in reality conditions because of the finite GBW of the OTA used in the adder, this adder also introduce excess loop delay that lead to peaking in the magnitude response of the NTF. Macro model simulation shows that an OTA with 20 MHz GBW and 60 dB DC-gain is suitable for implementation of the adder in order to mitigate the NTF peaking and achieve a good performance from the modulator.

Figure 17: Active adder with SC circuitry and Z^{-1} block



4. Modulator Front-End Noise Analysis

The performance of the modulator is degraded because the circuit noise at the modulator front – end is not attenuated. There are three source of noise for the noise of the front end: noise of the two input resistors, noise of the first OTA and eventually noise of R_{DAC}. The total in band noise caused by the two input resistors and two DAC resistors is:

$$\overline{v}_{R_1}^2 \approx 8kT(R_1 + R_{DAC})2f_\circ$$

Under condition $R_1=R_{DAC}$ the noise can be expressed as follow:

$$\overline{v}_{R_1}^2 \approx 32kTR_1 f_\circ \,|_{R_1=R_{DAC}}$$

Where $k = 1.38\times10^{-23}$ J/K (called Boltzmann's coefficient), T is the absolute temperature. In this design we choose R_1=7.5 kΩ. This value of R_1 generates thermal noise power about 100 dB lower than the full scale input signal.

In the OTA shown in Figure 12 the total in-band thermal noise is given by:

$$\overline{v}_{in,TH}^2 = \frac{16kT\gamma}{g_{m1,2}}(1+\frac{g_{m7,8}+g_{m9,10}}{g_{m1,2}})f_\circ$$

And the total in-band flicker noise of the OTA can be expressed as:

$$\overline{v}_{n,1/f}^2 = [\frac{2K_n}{(WL)_{1,2}C_{ox}f}+\frac{2K_p}{(WL)_{7,8}C_{ox}f}\cdot\frac{g_{m7,8}^2}{g_{m1,2}^2}+\frac{2K_p}{(WL)_{9,10}C_{ox}f}\cdot\frac{g_{m9,10}^2}{g_{m1,2}^2}]Ln(\frac{f_{\max}}{f_{\min}})$$

In the above equations, K represents Boltzmann coefficient, T represents absolute temperature and g_m represents the transconductance of the OTA. Also K_n and K_p represent the flicker noise coefficients of the NMOS and PMOS transistors respectively. According to the above equations the transconductance of $M_{1,2}$ should be maximized and the transconductance of $M_{7,8}$ and $M_{9,10}$ minimized.

4. SIMULATION RESULTS

The modulator was simulated in TSMC 0.18 µm CMOS technology. Figure 18 illustrates power spectral density of the Delta Sigma Modulator output. The number of samples is 2^{16} and the modulator operates at 3.2 MHz clock frequency for the 50 kHz bandwidth. Figure 19 shows both the system level and device level Dynamic Range of the designed Delta Sigma Modulator. According to this curve the modulator shows the peak SNDR of 102dB / 98dB @ -3dBFS in the system and circuit level respectively and the simulated DR is nearly 100dB in the circuit level. The power consumption is measured as 60 µw for 1.8 V supply voltage. Performance summary of the designed modulator and several state of the art micro power modulators are shown in Table 6.

Figure 18: Simulated power spectral density of modulator

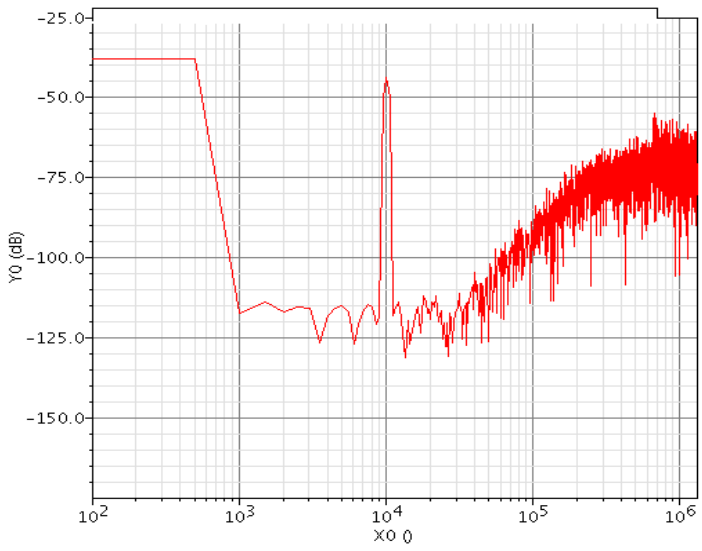


Figure 19: Dynamic range of the micro power CT-DSM in both system level and circuit level

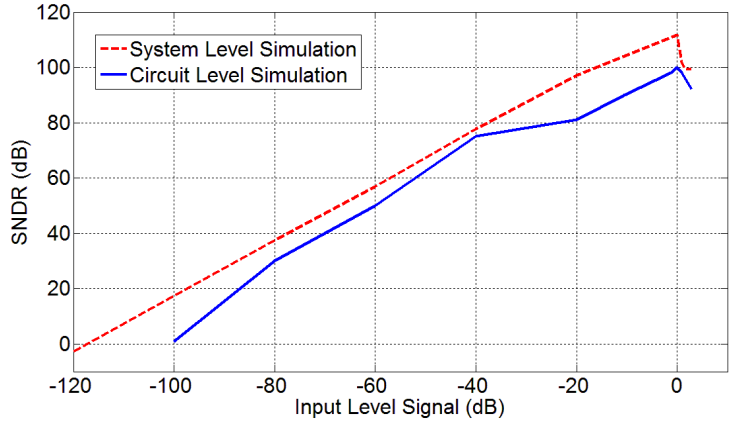


Table 6: Commonly used architecture OTAs

Ref	Structure	OSR	Signal bandwidth (kHz)	Sampling frequency (MHz)	SNDR (dB)	DR (dB)	Process (µm)	Supply voltage (V)	Power consumption (µW)
[2]	2nd order DT – 1bit quantizer	256	10	5	80	83	0.18	0.9	200
[3]	3rd order CT- 1bit quantizer	64	25	3.2	74	-	0.18	0.5	300
[4]	3rd order CT - CIFF	512	6	6.144	92.4	94.4	0.15	1.5	110
This work	Modified 3rd order CT – 1bit quantizer	32	50	3.2	98@-3dBFS	100	0.18	1.8	60

6. DISCUSSION AND CONCLUSION

A micro power Delta Sigma Modulator is presented in this article. Feed forward topology is opted in order to reducing the voltage swing of the integrators that lead to more power saving. A Noise Shaping Enhancement technique is applied for increasing the performance of the modulator without using active analog blocks, so more power saving can be reached. G_m over I_D method is used for design of analog building blocks in the sub-micron regime. Two OTAs are separately designed for first stage and other stages respectively. A Telescopic OTA has been used in the first integrator and Folded cascode OTA has been designed in the second and third integrators. This modulator has been simulated in a 0.18-µm TSMC CMOS technology. The simulated SNDR and DR are 98 dB and 100 dB, respectively and the modulator consumed only 60 µW. Although this modulator is designed as a part of CMOS analog front-end IC for portable biomedical applications but final results shows that the proposed modulator is more suitable for audio applications too.

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