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Recent Developments in the Hardware Architecture of H.264 Codec focusing on Intra Prediction Module

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ABSTRACT

Video coding has been of great research interest to the investigators for past decade and research capacity in video coding has been increased with the increased demand of high quality of video required for different purposes especially with the advent of mobile devices and their applications. H.264 is a next-generation video compression format. It is developed for use in high definition systems such as HDTV, Blu-ray and HD DVD as well as low resolution portable devices such as Sony's PSP and Apple's iPod. H.264 has been evolved as the standard for its better compression yet providing best quality. The hardware aspect of the H.264 codec is of prime importance and it is important to study the recent developments in the hardware architecture of the H.264 codec standard for better understanding of the system challenges and solutions for future development which is being presented in this paper.
KEYWORDS: H.264, intra prediction, FPGA, Parallelism.

1- INTRODUCTION

With rapid development of science and technology, popularity of high definition TV and telecommunications are creating greater needs for higher coding efficiency and fast computation hardware while keeping the power consumption low. Moreover, other transmission media such as Cable Modem, xDSL, or UMTS offer much lower data rates than broadcast channels, and enhanced coding efficiency can enable the transmission of more video channels or higher quality video representations within existing digital transmission capacities. The block diagram of H.264 codec is shown below in the figure 1.

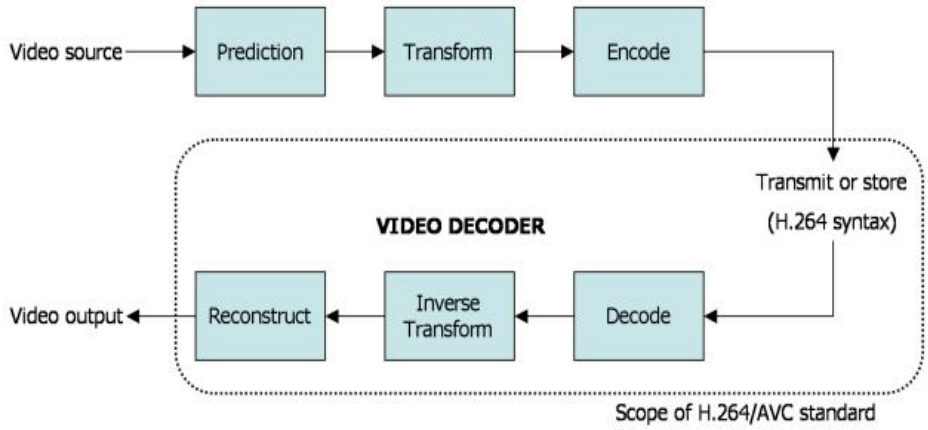

Fig. 1 H.264 Video Encoding and Decoding Process

The encoder processes a frame of video in units of a Macroblock (16x16 displayed pixels) that forms a prediction of the macroblock based on previously-coded data, which is obtained either from the current frame (intra prediction) or from other frames that have already been coded and transmitted (inter prediction). The encoder subtracts the prediction from the current macroblock to form a residual. In this paper some of the recent hardware architectures proposed are discussed specially focusing on the Intra Prediction module of the H.264 video encoder which holds an integral position in the overall structure of the H.264 Codec standard.

1. Recent H.264 Codec Hardware Architectures

The hardware architecture for H.264 encoder is complex and requires careful considerations of the hardware resources. This paper is about few latest techniques that have been developed in order of improving the efficiency of the discussed decoder in terms of computation, power consumption and reliability specifically from intra prediction of the encoder point of view which itself is an eminent part of the encoder.

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1.1. Intra Prediction Hardware Architectures

Four recent techniques for intra prediction architectures that have been developed for improving the efficiency of the H.264 codec are discussed.

1. A two-stage macroblock pipeline design, could encode SD (720 480) video at 30 fps at 54 MHz [1]. With this technique several H.264 intra-frame encoders have been proposed [2], [3]. The latest study reveals elimination of the plane mode prediction to speed up the encoding process, pro-posed an enhanced cost function to compensate video quality with a three-step heuristic intra-prediction algorithm [4] which skips to predict the modes that have lower probability to be the best mode. This design can encode 1080pHD video at 30 fps at 140 MHz and shows a 1.03% bit-rate increase and 0.11 dB PSNR drop on the average as compared to the H.264/AVC reference software Joint Model (JM) 8.6 . To have a low-power and high-performance H.264/AVC intra-frame encoder, a clock-gating technique was developed to reduce its power consumption [5]. It has also implemented a high-performance CABAC encoder to achieve better compression ratio. This can encode 1080pHD video at 30 fps without any PSNR drop while achieving better bit-rate saving running at 114 MHz and consumes only 23.56 mW. Four novel performance enhancement approaches 4x4 block parallel processing improving throughput of all engines, referenced column reconstructed first approach eliminating the bubble cycles between prediction of two 4x4 luma blocks, two-mode resource-sharing approach increases throughput of intraprediction unit and multi-bin processing approach simplifies the computation and increases the throughput of context-adaptive binary arithmetic coding encoder [5]. Figure 2 and Table 1 explains the phenomena discussed.

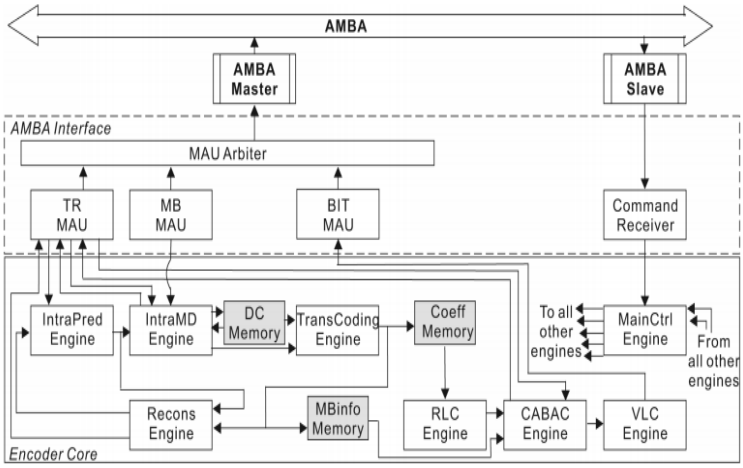

Fig. 2. Top Level Block Diagram

Table 1. Comparison with All previous Encoders

	[5]	[6]	[7]	[8]	[15]	Present study
Implementation						
Technology	TSMC 0.25 µm	UMC 0.18 µm	UMC 0.18 µm	TSMC 0.13 µm	TSMC 0.13 µm	TSMC 0.13 µm
Gate Count	85K	103K	75K	94.7K	212K	265.3K
On-chip memory (bytes)						
Single port	1K	2K	1.6K	1.84K	4.3K	2K
Dual port	0.7K	-	-	-	3.2K	1.2K
ROM	-	-	-	-	3.2K	3.2K
Power Consumption	-	-	-	-	95mW	23.56mW
Required working frequency						
1080pHD	-	-	-	140MHz	138 MHz	114 MHz
720pHD	-	117MHz	61 MHz	61 MHz	61 MHz	51 MHz
SD	54MHz	43 MHz	23 MHz	23 MHz	23 MHz	19 MHz
Video quality compared with JM						
Average PSNR drop (db)	0	0	0	0.11	0	0
Average bit-rate ratio						
JM with CAVLC	0%	+0.06%	+0.68%	+1.03%	-16%	-16%
JM with CABAC	-	-	-	-	0%	0%

2. Video compression is used in many applications. Recently, a new international standard for video compression, H.264 has better video compression efficiency than previously developed video compression standards and the achieved video compression efficiency in H.264 standard is not a result of any single feature but a blend of a number of encoding tools. Intra prediction algorithm used in the profile of H.264 standard is one of the tools [6]. As a result of this algorithm a prediction for a macro block based on spatial redundancy is obtained which promises better coding results than the intra prediction algorithms used in older video compression standards. However, computational complexity increases significantly with this coding gain. In quest to reduce this amount of computation and power consumption one of the techniques developed is a pixel equality based technique [8]. It compares the pixels used in all prediction equations of an intra prediction mode. If the pixels are found to be equal in all equations of a prediction mode, the predicted pixels by this mode are equal to these pixels, simplifying prediction equations to a constant value and prediction calculations for this mode become unnecessary such as for H.264 intra 4x4 luminance prediction modes which have identical equations and calculating these common equations for each mode is unnecessary. The hardware architecture for an efficient H.264 4x4 intra prediction hardware is implemented in verilog HDL and the RTL code is verified to work at 50 MHz in a Virtex II FPGA [9]. This technique reduced the power consumption of this hardware on this FPGA up to 13.7%. The amount of computations performed by H.264 intra prediction algorithm is reduced significantly without any PSNR and bitrate loss. Figure 3 and table 2 and 3 depicts the discussed architecture.

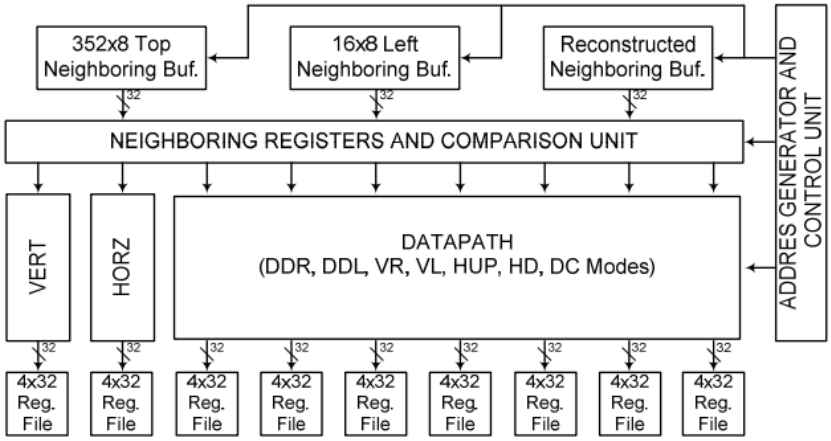

Fig. 3. 4x4 Intra Prediction Hardware Architecture

Table 2. Computation Reduction

reduction		Reduction by PECR technique proposed in[3]				Reduction by data reuse and PECR technique			
		Addition reduction		Shift reduction		Addition reduction		Shift	
	QP	#	%	#	%	#	%	#	%
Foreman	28	246939	27.9	146816	27.7	662350	74.9	408181	77.1
	35	365863	41.4	216263	40.9	722417	81.7	440934	83.3
	42	459269	51.9	269710	50.9	758590	85.8	460350	87.0
Akiyo	28	386890	43.8	229707	43.4	722826	81.8	441285	83.4
	35	461728	52.2	273099	51.6	760791	86.0	461740	87.3
	42	521463	58.9	306887	57.9	786741	89.0	475764	89.9
M&D	28	359883	40.7	214067	40.5	707595	80.0	432743	81.8
	35	469840	53.1	278673	52.6	761340	86.1	462156	87.3
	42	539033	60.9	317345	59.9	790203	89.4	477466	90.2

Table 3. Power Consumption Reduction

Frame	Category	Power(mW)		
		4x4 intra prediction Hardware	4x4 intra prediction Hardware with power Red. Tech.	Reduction (%)
Forman	Clock	24	21	12.5
	Logic	7.0379	5.5934	20.5
	Signal	23.1136	21.0505	8.90
	Total	54.152	47.644	12.0
Akiyo	Clock	24	21	12.5
	Logic	6.8965	5.3359	22.6
	Signal	22.3333	19.7146	11.7
	Total	53.230	46.051	13.5
Mother Daughter	Clock	24	21	12.5
	Logic	6.833	5.224	23.5
	Signal	22.184	19.525	12.0
	Total	53.017	45.749	13.7

3. To speed up H.264 intra frame coding, these algorithms are implemented by dedicated hardware accelerators and in such efforts these hardware resources are often wasted if intra predictions and reconstructions for 4x4 blocks are serialized. To overcome a hardware waste, a pipelined execution of the intra predictions and reconstructions of 4x4 blocks which has the processing orders of 4x4 intra predictions are derived for both encoding and decoding, respectively, in order to reduce the dependencies between consecutively processed blocks and minimize pipeline stalls. This pipelined execution of 4x4 intra predictions for encoding is incorporated with the other intra frame encoding operations with an efficient scheduling to allow these other operations to be executed in parallel with intra prediction. Comparison shows that the best previous work for intra frame coding [10], the execution time is decreased by 41% even with reduced hardware resources [11]. The pipelined execution of Luma 4x4 intra prediction, that is the computation bottleneck of intra frame encoding mainly achieves the speed. With the proposed pipelined execution, the compression efficiency is almost the same to the original JM reference software and the Luma 4x4 intra prediction is efficiently overlapped with integer transform, quantization, inverse integer transform, and inverse quantization for 4x4 Luma blocks, 16x16 Luma block as well as 8x8 Chroma blocks with no extra cycles in addition to the execution time of 4x4 Luma blocks are required to process these other computations. Table 4 explains the architecture from different efficiency parameters.

Table 4. Execution Time, Bit Rate, PSNR and Time Reduction Comparison

TABLE 1 EXECUTION TIME COMPARISON

METHOD	PROPESED	Suh .et .al [1]	Haung .el .Al [2]
CYCLES	548	927	1280

TABLE 2 BITRATE COMPARISON

Sequence	Original H.264 without pipeline	Original H.264 + Full pipeline	Proposed order + Full pipeline	Proposed order +partial pipeline
Akiyo	78,914	84,689	80,678	79,044
Mother & Daughter	86,563	92,628	88,978	87,286
Stefan	486,478	498,238	490,310	487,171
Forman	186,929	203,184	192,396	187,003

TABLE 3 PSNR COMPARISON

Sequence	Original H.264 without pipeline	Original H.264 + Full pipeline	Proposed order + Full pipeline	Proposed order + partial pipeline
Akiyo	35,990	35,960	35,989	35,991
Mother & Daughter	38,045	37,928	38,014	38,032
Stefan	34,223	34,195	34,212	34,231
Forman	37,365	37,344	37,368	37,342

TABLE 4 TIME REDUCTION COMPARISON

Sequence	Original order	Proposed order
Forman	6786	1535
Mother & Daughter	5770	1302
Akiyo	4473	1087
Stefan	6879	1596
Average	5977	1380

4. By analyzing the problems causing unnecessary processing cycles or hardware resource, a four-parallel intra prediction engine is and integrated into an H.264/AVC baseline encoder for HDTV applications [12]. It gives result 47.9% to 67.5% cycle-reduction with near 100% utilization under real chip environment. The designed four-parallel intra prediction architecture applied with four optimization schemes namely Category-Level Interleaved Scheme (CLIS) eliminates the bubble cycles of I4MB reconstruction. Mode-Level Scheduling (MLS) and Early Data Preparation Scheme (EDPS) rearrange the processing sequence of intra modes [13]. The earlier low-complexity modes hardware resource is used to deal with the computation of later high-load modes. With the increase in the hardware utilization,the processing cycles is also reduced. In addition, Stage-Level Partial Distortion Elimination (SLPDE) is induced to skip the calculation of unnecessary intra modes. This architecture has been integrated into an H.264/AVC baseline encoder for HDTV applications and has been verified to be feasible under system consideration [6]. Comparison with four schemes is shown in table 5.

Table 5. Comarison with Four Schemes

	Processing cycle per MB(cycle)	Reduction Rate (%)
Original	(36+4+20)*16+(26)*16=1376	0
CLIS only	(36+4)*16+(26)*16=1056	23.5
MLS only	(36+4+16)*16+(26)*16=1312	4.7
EDOS only	(36+4+20)*16+(16)*16=1216	11.6
Apply three scheme	(36+4+16)*16=896	34.9

2. Other Modules Architectures

Some of the recent developments in various hardware architectural components of the H.264 codec for better performance are discussed.

The comparison between an automated and a custom-design approach in terms of the design time, throughput requirements it is observed that a fully automated design cycle should be much shorter than a fully custom design cycle and also has lower performance a lower cast. Further, the study shows that full automation against semi-customization, the fully automated design concerns a software MPSoC implementation in which the processing elements are programmable cores (microblazes), whereas the custom design is a hardware implementation in which the processing elements are IP cores that are not fully dedicated [14].

The implementation of the application on an MPSoC plat-form based on the DAEDALUS flow brings down design and validation time and In fact, the whole design is correct by construction. However, this comes at a cost because of the construction of the SAN LP application specification which is a time consuming manual process, and the DAEDALUS specific platform architecture is always in terms of computational components, and a communication, synchro-nization, and storage infrastructure composed from library components [14].

An IP-core and/or stand-alone solution targeting to low area applications encoder architecture achieves maximum throughput of 30 frames/sec with frame size 1024x768 [15].

By generating multiple RTL designs for a complex IP block (H.264), an inexpensive, low-performance decoder targeting mobile platforms which can be implemented in 2.22 mm2 and a number of high-performance decoders capable of decoding 1080p video at more than 60 fps that takes only twice that Area, can be achieved [16].

An AMBA-based IP that can perform the H.264 transform and quantization operations for video compression/decompression in which the core of the IP is the transform and quantization circuit optimized for area. IP allows the user to specify the options such as how long the bus may be occupied by the IP, where the video data are stored in the external memory, and so on [17]. The platform board with Xilinx FPGA and ARM9 processor is built and demonstrated the correct operations. An MPW chip with our IP was fabricated using 0.25ptm standard cells to prove its AMBA-compliant operations on silicon [17].

When it comes to the memory performance of SVC, the frame-level encoding enjoys the minimal internal memory storage and the lowest external memory bandwidth. With other improvements in temporal and quality domain, the overall requirement of external memory bandwidth could be further decreased over 53% [18].

An in depth investigation into the design spaces of inter-prediction (IME and FME) parallelism, macro-block (MB) pipelining, and search-range buffering shows that get the most area efficient design under given specifications in cluding resolution, frame rate, reference frame size an multiple reference frames with flexibility an usefulness [19].

3. Conclusion

H.264 / AVC is considered as an industry standard for video compression, and it involves the process of converting digital video into a format that takes up less capacity when it is stored or transmitted. Video compression or video coding is an essential technology for applications such as digital television, DVD and Blu-Ray disks, mobile TV, videoconferencing and internet video streaming. The hardware architecture for the H.264 codec is of great importance to study as it has been observed in the study that by optimizing the hardware for

H.264 codec the efficiency obtained is significant and provides scope for future work such as making the reconfigurable hardware for the encoder will be one of the best solutions where the system needs to react with varying environment.

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