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Design of a Nanometric Fault Tolerant Reversible Multiplier Circuit

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ABSTRACT

Reversible logic circuits have many applications in quantum computing, nanotechnology and low power CMOS design, optical information processing. In spite of irreversible circuits, reversible circuits are not power-dissipated, so they are very noteworthy. In this study we designed a reversible multiplying circuit which is also fault tolerant. This circuit was constructed by using of parity preserve gates and applicable for multiplying of two 4-bite digits. Several reversible multiplier circuits have been designed but reversible multiplier circuits that also been fault tolerant has not yet been designed so we proceeded to it and also we show that MIG gate has a quantum cost of only 7. All the scales are in the nanometric area.
KEY WORDS: reversible logic, multiplier, fault tolerant, parity preservation, nanometric scales.

1. INTRODUCTION

One of the most important issues in VLSI circuit designing is reducing the power dissipation. Circuit designing as irreversible, leads to power dissipation as heat that due to the loss of information. In computing systems for every bit of lost information KTLn2 joules of energy is lost (Landauer, 1961) where $K=1.3806505*10^{-23} m^2 kgs^{-2} K^{-1}$ is Boltzmann's constant and T is the temperature where the operation performed. So Bennett indicated that if the reversible circuit can be use will not lose information. So much power dissipation would be zero. (Bennett, 1973).

Reversible circuits have many applications including low power CMOS design, digital signal processing, nanotechnology, optical computing. Reversible circuits are the circuits that composed of reversible gates. Reversible gates are the gates that the numbers of input vectors are equal to output vectors and can be found on the input, output vectors and also set the output, input vectors gain (Perkowski et al., 2001; Perkowski et al., 2001b; Thapliyal and Srinivas, 2005). Two limits for the reversible circuit are that they are not allowed feedback and fan out (Perkowski et al., 2001). Feed back means that we have not loop and fan out also means that an output can not use more than once.

An appropriate reversible circuit will be obtained when following factors to be considered: number of gates, number of garbage outputs, number of constant inputs and Total quantum cost (QC). Whatever these factors much less is better. Constant input vectors means the input that the value of it, is given 0 or 1. Number of gates presents number of gates used in the circuit. Garbage output also means that gate output is not used (Thapliyal and Srinivas, 2005). Quantum Cost (QC) of reversible circuit is obtained by calculating of number of 1*1 or 2*2 reversible gates or quantum gates witch are used in circuit designing.

Reversible circuits can also designed as fault tolerant, because these systems can continue properly their own calculations while an error occurs in one of the components of systems.

In order that the system to be fault tolerant it is necessary that gates are used to be parity preserve. Parity checking is one of the conventional methods to detect errors in digital logic systems. Parity preserve is the gate that the parity of input and output vectors of them is the same. So build the reversible circuits and fault tolerant reversible circuits more complicated than building conventional circuits.

Hitherto several reversible multiplier circuits have been designed but reversible multiplier circuits that also been fault tolerant has not yet been designed so we proceeded to it.

2. Background

A reversible gate that has k input surly it has k output which is called k×k gate. Now some reversible gates are followed:

2.1. Feynman Gate (FG)

Feynman gate is a 2×2 gate that produces logical functions of P=A and Q=A ⊕ B. (Feynman, 1985). This gate is shown in Fig. 1. By using of this gate we can copy a bite and it is used as a NOT gate. Because as mentioned above, in reversible circuit, fan out is not allowable, so Feynman gate can

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be used for this purpose as if B is set to be zero, P=A and Q=A output vectors are produced, also if A input is set to be one, P=1 and Q=B′ output vectors are generated. Quantum cost of FG is 1.

Fig.1. Two symbols of Feynman gate

2.2. Toffoli Gate (TG)

Fig. 2 presents that Toffoli is a 3×3 gate which A, B and C are input vectors of it and output vectors of Toffoli gate produce P=A, Q=B and R=AB⊕C logical functions (Toffoli, 1980). In this gate if C input vector is set to be zero, output vector R of it be AB. Quantum cost of TG is equal to 5 because this gate is constructible by using of five 2×2 gates.

Fig.2. Two symbols of toffoli gate

2.3. Fredkin Gate (FRG)

Fredkin gate is a 3×3 gate (Fredkin and Toffoli, 1982). Input vectors of it are A, B and C. As shown in Fig.3. P = A, Q=A′B⊕ AC and R=A′B⊕ AC are produced logical functions by FRG. Also the Fig. shows that this gate is used as swap action as while A input vector is set to be zero, locale of A and B are changed. It should be noted that quantum cost of this gate is 5.

Fig.3. Two symbols of Fredkin gate

2.4. Feynman Double Gate (F2G)

F2G that is shown in Fig. 4 is sample of 3×3 gate (Parhami, 2006). It has A, B and C input vectors. As well as output vectors of F2G produce P=A, Q=A⊕ B and R=A⊕ C logical functions. The difference of this gate with FG is in the number of input and output vectors which one input and one output is added. Quantum cost of F2G gate is equal to 2.

Fig.4. Two symbols of Feynman Double gate

2.5. New Fault Tolerant Gate(NFT)

NFT gate is shown in Fig. 5. which it is a 3×3 gate that composed of A,B and C input vectors and output vectors of it, produce P = A⊕ B, Q = B′ C ⊕ AC′ and R=BC⊕ AC′ logical functions. This gate has been presented which it can implement all of the AND, XOR, NOT, NAND, XNOR, NOR logical functions. Quantum cost of NFT gate is 5. (Haghparast and Navi, 2008)

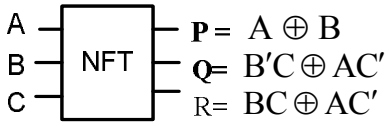

Fig.5. NFT gate

2.6. Islam Gate (IG)

4×4 IG gate is involved A, B, C and D input vectors (Islam and Rahman, 2009). As realized with regard to Fig. 6, IG's outputs are formed P=A, Q=AB ⊕ C and S= BD ⊕ B′ (A ⊕ D) logical functions. Quantum cost of Islam Gate is 7. (Haghparast and Navi, 2010)

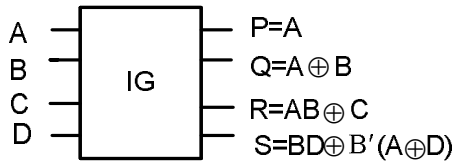

Fig.6: Islam Gate

2.7. Modified IG gate (MIG)

MIG as shown in Fig. 7 is a 4×4 gate. It includes A, B, C and D input vectors. Output vectors of MIG produce P=A, Q=A ⊕ B, R=AB ⊕ C and S=AB′ ⊕ D logical functions. (Islam and Rahman, 2009b).

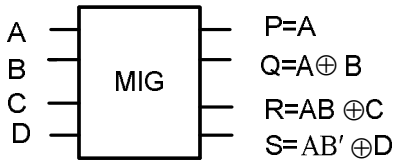

Fig.7: MIG Gate

2.8. Parity preserving gates

With consideration of restricts of reversible gates, such as not allowable fan out, there are some problems related to use of standard methods of error detection. Because consequences of application of these methods cause to increase of garbage outputs numbers parity checking is commonly use for error detecting. Therefore parity preserve will be required. Parity preserve is the gates that the parity of inputs and outputs of them are the same (Parhami, 2006).

FRG, F2G, NFT, IG and MIG gates of presented gates in previous sections are parity preserve. Elaborate in FRG, A ⊕ B ⊕ C=P ⊕ Q ⊕ R, in F2G A ⊕ B ⊕ C=P ⊕ Q ⊕ R, in NFT, A ⊕ B ⊕ C=P ⊕ Q ⊕ R, in IG, A ⊕ B ⊕ C ⊕ D=P ⊕ Q ⊕ R ⊕ S, and in MIG, A ⊕ B ⊕ C ⊕ D=P ⊕ Q ⊕ R ⊕ S are established. IG and MIG are parity preserve gates hence as shown in Fig. 8 the full adder designed via two IG gates or two MIG gates will be parity preserve (Islam and Rahman, 2009; Islam and Rahman, 2009b).

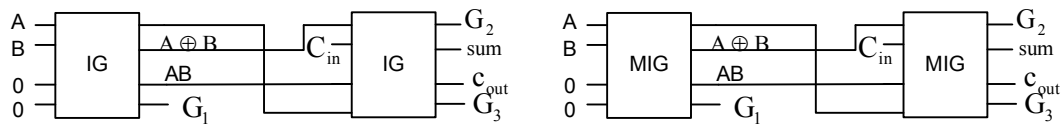

Fig.8. Fault tolerant reversible full adder circuit includes: (a) two IG gates (b) two MIG gates (Islam and Rahman, 2009; Islam and Rahman, 2009b).

3. Our proposed quantum realization of parity preserving reversible MIG Gate

One of criteria for assessment of reversible circuit is quantum cost of circuit. Therefore in this section quantum cost of the MIG Gate is proposed. The proposed circuit is shown in Fig. 9. As be mentioned quantum cost of circuit is equal to the number of 1×1 or 2×2 reversible gates or quantum gates. For example FG, V, V^+ gates are some quantum gates, some properties of V and V^+ gates are following.

$$\begin{cases} V \times V = NOT \\ V \times V^{+} = V^{+} \times V = I \\ V^{+} \times V^{+} = NOT \end{cases}$$

These relationship are established while V and V^{+} gates be active, and these gates are active when the control line of them is 1. If these gates are not active, input of them is transported to output. As shown in Fig. 9 the P output is equal to A input and Q output is equal to $A \oplus B$. The R output is described by V and V^{+} quantum gates, also S output is obtained by $R \oplus P \oplus C \oplus D$. As relationship $R \oplus P \oplus C \oplus D = AB' \oplus C$ is established. Therefore the quantum cost of proposed realization is only 7. Trust table of Fig. 9 is presented in Table1.

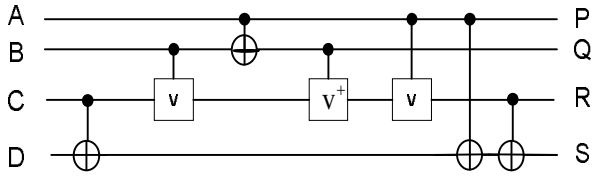

Fig. 9: Our proposed equivalent quantum representation of parity preserving reversible MIG gate.

Table1. Trust table of proposed equivalent quantum representation of parity preserving reversible MIG gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	**0**
0	0	0	1	0	0	0	**1**
0	0	1	0	0	0	1	**0**
0	0	1	1	0	0	1	**1**
0	1	0	0	0	1	0	**0**
0	1	0	1	0	1	0	**1**
0	1	1	0	0	1	1	**0**
0	1	1	1	0	1	1	**1**
1	0	0	0	1	1	0	**1**
1	0	0	1	1	1	0	**0**
1	0	1	0	1	1	1	**1**
1	0	1	1	1	1	1	**0**
1	1	0	0	1	0	1	**0**
1	1	0	1	1	0	1	**1**
1	1	1	0	1	0	0	**0**
1	**1**	**1**	**1**	**1**	**0**	**0**	**1**

4. Proposed fault tolerant reversible multiplier circuit

Our proposed circuit is parity preserve 4×4 multiplier. It has been designed in two parts. Multiplying of two digits is shown in Fig. 10.

			×	x_3	x_2	x_1	x_0
				y_3	y_2	y_1	y_0
				x_3y_0	x_2y_0	x_1y_0	x_0y_0
			x_3y_1	x_2y_1	x_1y_1	x_0y_1	
		x_3y_2	x_2y_2	x_1y_2	x_0y_2		
	x_3y_3	x_2y_3	x_1y_3	x_0y_3			
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Fig.10. Partial products in a 4×4 multiplication

First part of multiplier circuit, which is shown in Fig. 11, is used for producing of $x_i y_j$ functions which is shown in Fig. 10. By using of parity preserve 3×3 FRG, this part of multiplier has been designed. Second portion of multiplier that is shown in Fig. 12 consists of some parity preserve full adders and half adders that Fig. 8.b is placed instead of full adders and half adders are placed by MIG gates. Finally multiplying of two 4-bit digits result will be generated. (p_0 to p_6).

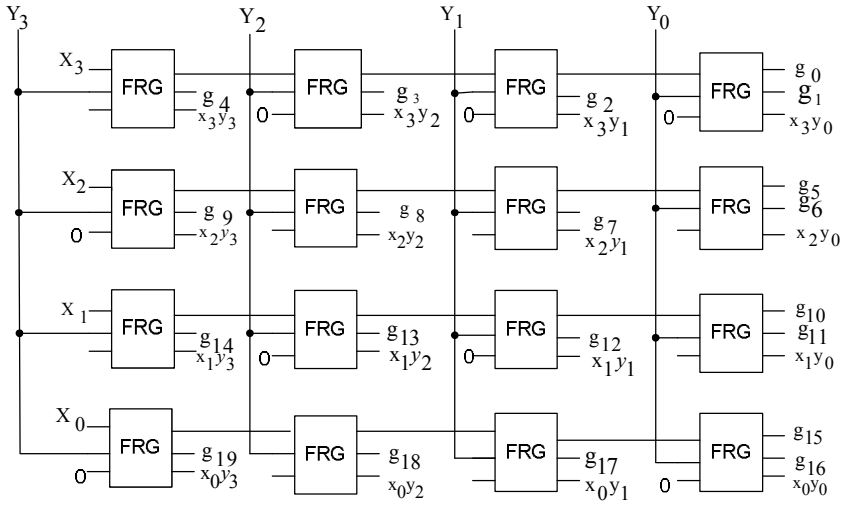

Fig.11.reversible partial products generation circuit using fredkin gates

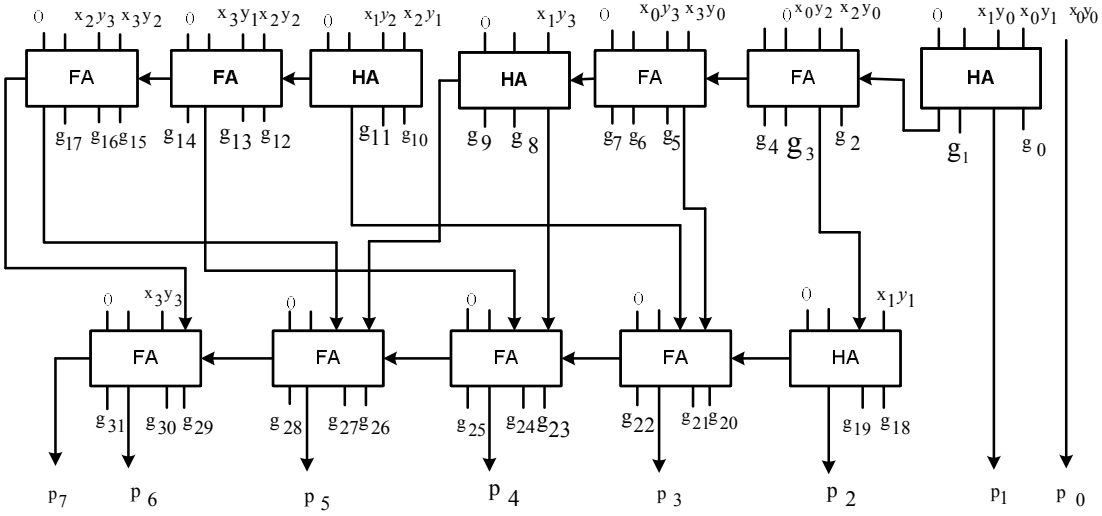

Fig.12. Our proposed 4×4 fault tolerant reversible multiplier circuits uses MIG full adder and half adder

Table2. Comparative experimental results of common reversible multiplier circuits with the proposed fault tolerant reversible multiplier circuit.

Reversible Multiplier	Fault Tolerant Property	No. of gates	No. of Garbage Output	Total Quantum Cost	No. of Constant Inputs	Totla Logical Calculations
This work*	Yes	48	64	244	52	116α+104β+36γ
(Haghparast et al., 2009) (Design 1)	No	28	28	137	28	71α+36β
(Haghparast et al., 2009) (Design 2)	No	36	28	153	28	63α+36β
(Haghparast et al., 2008)	No	52	52	152	52	104α+36β
(Shams et al., 2008)	No	52	56	244	56	116α+52β+36γ
(Thaplyal and Srinivas, 2006)	No	53	58	286	58	134α+103β+71γ
(Thaplyal et al., 2005)	No	64	56	236	55	104α+100β+68γ

5. Assessment of proposed circuit

Comparative experimental results of common reversible multiplier circuits with fault tolerant reversible multiplier circuit are shown in Table2.

Hardware complexity is one of criteria for surveying the reversible circuits which calculates the numbers of XORs, ANDs and NOTs that used in output vectors of gates. These are presented by α, β and γ respectively.

FRG and MIG are the gates that used in our proposed circuit. FRG gate consists of two XOR, four ANDs and two NOTs also MIG gate has three XORs, two ANDs and one NOT. So in general case the total logical calculation is: T= 116 α+104 β+36 γ.

Other criteria for assessment of circuits are number of gates, number of constant input, number of garbage output and quantum cost. Their calculating is following: number of gates: these criteria introduce the number of gates that used in circuit. Our proposed circuit consists of 16 FRG and 20 MIG gates and 12 F2G gates, therefore it has 48 gates. Number of constant input means the inputs that set to be 1 or 0 constant value. In used FRG gates one input of them is set to be zero and in MIG gate which used as half adder has two constant input and set to be zero. Also in full adder there are two constant inputs hence in general case it will be $1\times16+2\times4+2\times8+1\times12=52$.

As well as to calculate the numbers of garbage outputs, it is considered that each of FRGs is consists of two garbage outputs and each of MIG gates as a half adder has two garbage outputs and as a full adder has three garbage outputs. So in general case the numbers of garbage output of circuit are equal to be $20+2\times4+3\times8+1\times12=64$.

To calculate the quantum cost of circuit, it is noted that the quantum cost of FRG is 5. As shown in Fig. 9 the quantum cost of MIG gate is 7.
Therefore quantum cost of circuit is equal to be $QC=5\times16+7\times20+12\times2=244$.

6. Conclusions

In this paper we presented a fault tolerant reversible 4×4 multiplier circuit. For construction of it parity preserve FRG and MIG gates were used. Multiplier circuit was designed in two parts. In second part of circuit MIG gates can be used instead of half adders and full adders. Also we show that MIG gate has a quantum cost of only 7. More studies are necessary by employing some techniques to reduce the constant inputs, garbage outputs and quantum cost of this circuit. All the circuits have nanometric scales.

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