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Programmable Trapezoidal and Gaussian Membership Function Generator

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ABSTRACT

This study focuses on generating various shapes of membership function circuit (MFC) with digital output. First a flash ADC has designed and then in order to generate digital output which can easily support digital environment, we applied this converter to the output of MFCs. Trapezoidal and Gaussian are more common shapes of MFCs. To obtain programmable trapezoidal shape and to achieve best performance, MFC and proposed digital conversion can be done contemporary. By changing some switches we can also generate programmable triangular shape, Z-shape, and S-shape. To obtain programmable Gaussian shape applicable in data classification, a simple MFC has been used. Compatible with digital circuit is great advantage of proposed circuits implemented in Current mode. Simulations in 0.35μm standard CMOS technology show the performance of circuits are given.

Keywords: triangular, Gaussian, current-mode, flash

INTRODUCTION

Fuzzy logic controllers are in general considered being applicable to plants that are mathematically poorly understood and where the experienced human operators are available. Structures for integrated circuits realization of fuzzy controllers are: analog (Guo et al., 1996; Vidal et al., 1997; Weiwei et al.,2008; Yamakawa 2011) , digital (Patyra et al.,1996; Geun et al.,2011; Mohammad et al.,2009) and mixed analog /digital (Vidal et al.,1998; Dualibel et al.,2001; Bouras et al.,1998). Each one of them has some advantages and disadvantages that make it suitable for a special purpose. Current-mode is getting popularity due to its high speed, low power consumption, large dynamic range, natural form of addition and subtraction and reduced system chip size. CMOS based technology is preferred over BJT technology (Liviu et al.,2003) due to high component density, low power consumption and easy fabrication process. Hence we choose a CMOS based current-mode to release membership function circuit (MFC).

A key element in the design of a high speed fuzzy processor is the availability of a high speed MFC to allow maximum processor speed. Analog fuzzifiers (or membership function circuits) with fully independent, electronically and continuously adjustable characteristics have been reported that allow high speed fuzzification, but they do not interface easily with digital systems. However, not, much has been said about the design of MFCs with digital outputs. Great benefits of digital data is its capable to saving and keeping data and also it can support other digital environments and its signals are much robust against noise and distortions. In application of fuzzy controllers, for implementing membership circuit, fully digital circuits (gate level) increase its hardware and complexity. But transistor level is better approach with low hardware and low power. Hence at this paper we have generated digital output of MFC with analog circuit base on transistor level by using novel method that we will explain in future sections.

The reminder of this study is organized as follows. In Section 2 we have looked at previous related works. Section 3 describes the method of generating programmable trapezoidal shape. Section 4 shows method of generating Gaussian shape. System simulation is shown in section 5. Finally the conclusion is given in the last section.

A brief study of previous works

Membership function generator (MFG) is an important concept used in the fuzzy logic theory. It is the process of converting a crisp value into a fuzzy value. The conversion is actually the incorporation of fuzziness, uncertainty, vagueness or ambiguity in the crisp quantity. In the real world the quantities which look crisp, actually carry a considerable amount of uncertainty or vagueness. The researchers have developed various MFG for the fuzzy processors they have developed. The design of a MFG depended on the particular application their fuzzy processor is being applied. In (Gabrielli et al.,1997) an efficient VLSI design of a 4 input high speed fuzzy processor has done. The MFG block of their design possesses four memories which store four points of a trapezoidal membership function. An efficient architecture of a fuzzy processor with parallel rule execution has been designed in (Jacomet et al., 1994). A high performance is achieved in this architecture due to the use of parallel processing. This method results in high flexibility in defining membership function. Further, the architecture employs a maximum 2 overlapping membership function, resulting in small memory.

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A circuit with Gaussian and Triangular functions suitable for analog neural networks has proposed in (Abuelma'ati et al., 2006). In that work, the centre, width, and peak amplitude of the dc transfer characteristic of shapes can be independently controlled. In (Tokmakci et al., 2002) a MFC based on simple OTA structure and current-mode maximum circuits has presented. This MFC implements basic four membership functions (trapezoidal, triangle, Z-shape and S-shape). The characteristics (width, height, slope and position) of the implemented membership functions are easily adjustable and it is suitable for current-mode fuzzy hardware. A digital design of a Gaussian membership function circuit is presented in (Basterretxea et al., 2006). In their work, positioning of the function on the universe of discourse can be selected, and its width or variance can be adjusted. The circuit is therefore suitable for implementing digital neuro-fuzzy systems with learning capabilities. Since they implemented their idea with digital circuits, it needs heavy hardware. A low-voltage CMOS circuit for the implementation of triangular/trapezoidal transconductance functions with programmable characteristics has been introduced in (Kachare et al., 2005). The circuit can be used as a building block for programmable PWL function approximation, for the implementation of VLSI analog neurofuzzy systems, and for high speed folding ADCs. The circuit has independently adjustable height, slope (both with constant width and with constant height), canter position, and width of the trapezoidal function. As we reviewed previous papers, we noticed lack of analog MFC with digital output for wide verity shapes. Therefor at this study we look at proposed circuits for this purpose.

Programmable Trapezoidal Shape

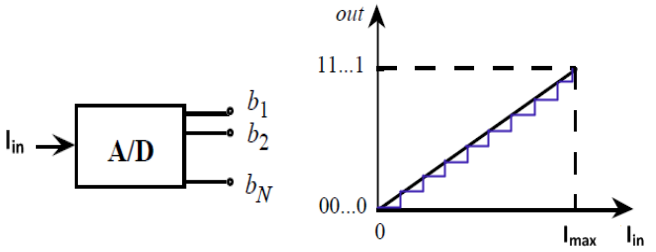

Fig. 1: Symbol and transfer characteristic of a conventional A/D converter.

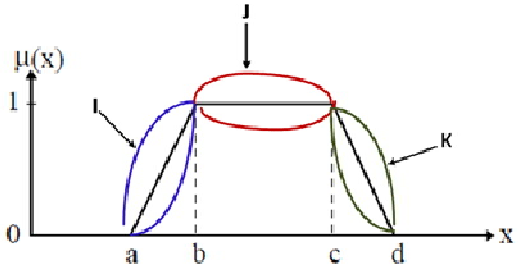

Fig.2: a shape with trapezoidal characteristic

Fig. 1 shows the transfer characteristic of an A/D converter. Design parameters are: the full-scale range, I_{max}, and the number of bits. Since we are going to obtain digital trapezoidal shape, we have two choices: one is upgrade this shape to match with trapezoidal shape another is to analysis trapezoidal shape based on this conventional converter. Let us choice the second solution.

The standard method for defining one-dimensional trapezoidal membership functions is with four points a, b, c, and d, as shown in Fig. 2. This Fig. illustrates an example of trapezoidal characteristic. Instead of the full-scale range I_{max}, it has four parameters, a, b, c and d, that define the slope and the offset of the two oblique edges. To obtain this fig, let us divide it in two portions as shown in fig.3.

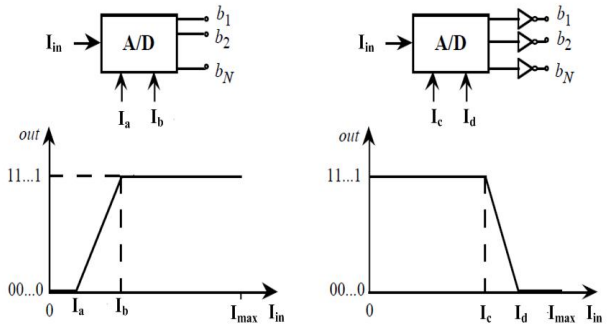

Fig. 3: Implementation of the membership function with two A/D converters.

Fig.3 left can be obtained through a shifting and a compression of the A/D transfer characteristic in the Interval [I_a, I_b], In the same way, through a compression in the interval [I_c, I_d] and through a mirroring, we can obtain the second part (i. e., the falling edge) of the transfer characteristic. To achieve total trapezoidal shape we can combine all together as shown in fig.4.

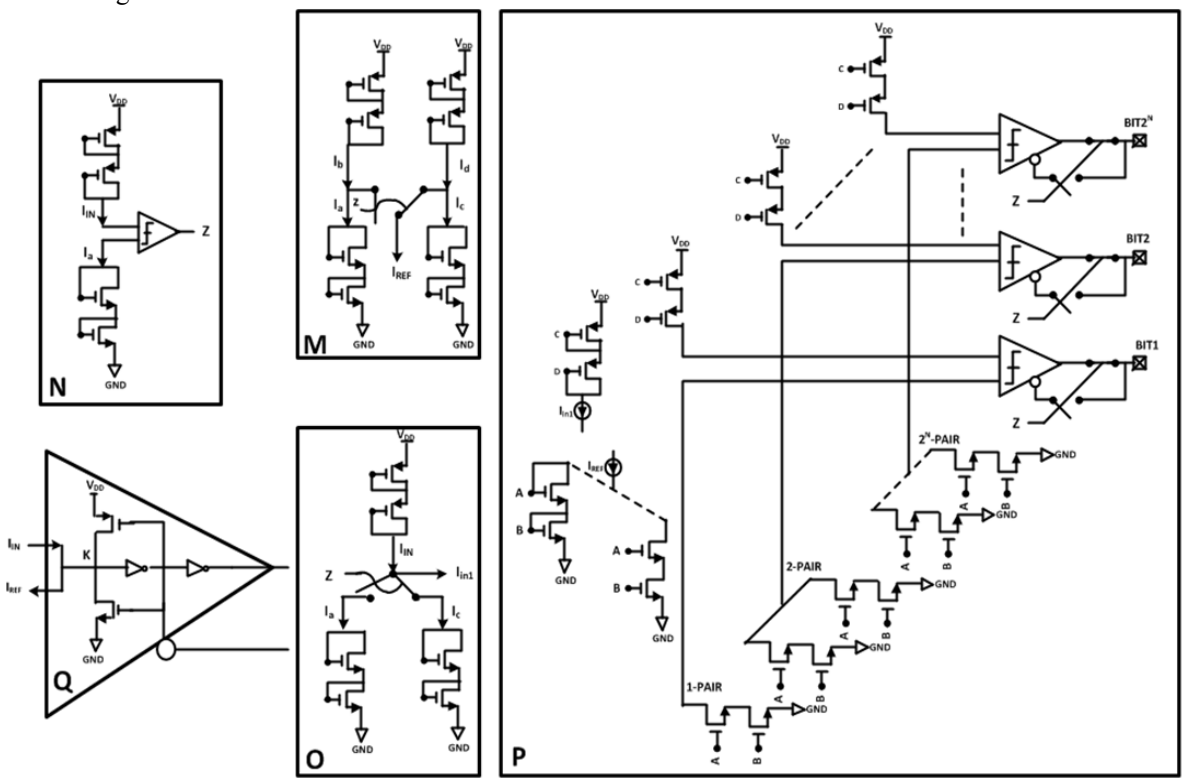

fig.4: main block of programmable trapezoidal shape

In this fig.4, part P shows the general architecture of an N-bit Current-mode FLASH A/D Converter. To avoid more complication we have shown connection with A, B, C, and D terms. It is composed of 2^N current-mode comparators. In this figure, the input signal (Iin) is copied and distributed to all the comparators using identical PMOS current mirrors. A reference input current is also necessary which determines the ADC input range. The reference signal (Iref) is divided to 2^N pairs of NMOS and before distributed to all the comparators gradually increases using identical NMOS current mirrors. For its internal comparators we have used fig.1.(Q). It is made up of NMOS and PMOS transistors and two inverters. At input of this converter (node k), I_{in} is compared to I_{ref} , If $I_{in} > I_{ref}$ the voltage of node k increases and last output of two inverters shows "1" logic, otherwise it switches to "o" logic. The output of inverter is known as thermometer and should convert to binary.

To achieve high performance and low area we can combine flash ADC and membership function block together like (Gianluca et al., 2002; Di Cataldo et al., 1996). They used ADC using successive approximation method but here we take advantages of Flash method and we obtained high speed MFC. For implementing this idea, let us to see fig.2 again. It shows trapezoidal membership functions, we have shown three parts of this shape in I, J, and K terms. To convert first piece of this shape (I) we just need this linear curve to shift this curve until point a lies on zero point of two dimensional diagram of membership function. At this point we can convert this part of shape to digital data like conventional method of ADC. Fig.2(I). Par J of this shape also acts as end of previous shape.

The last part fig.2 (K) is obtained with the same technique and by complementing all the output bits (mirroring operation) in the interval [I_c, I_d]. Circuits N, M, and O in fig.4 assemble suitable control for both input and reference currents.

Programmable Gaussian Shape

Data classification is an application where neural algorithms show promising capabilities. In many neural classification algorithms, the decision on the class associated to an input pattern is based on the comparison of the different probabilities to belong to each possible class. In the associated calculations, the probability density functions are needed. In many cases these functions can be modeled by normal distributions. Even though these algorithms can be conveniently implemented on workstations, in real time, portable and other space or power constrained applications, dedicated hardware implementation is a promising solution. The Gaussian distribution is usually quite good approximation for a class model shape in a suitably selected feature space. It is a mathematically sound function and extends easily to multiple dimensions. In the Gaussian distribution lies an assumption that the class model is truly a model of one basic class. Trapezoidal waveform and Gaussian waveform are both the usual membership functions.

However, Gaussian shape membership function can obtain smoother transient response and facilitate the analog implementations. Other approaches to implement in CMOS technologies the Gaussian function in weak inversion operation (Roberts et al.,1991) or as a piece-wise linear approximation (Gregorian et al., 1983) have been reported. A circuit that generates a true Gaussian form in weak inversion using only five transistors and can approximate the function also in strong inversion operation mode reported in (Madrenas et al., 1996). That work was not so accurate.

It is hard to implement the exact Gaussian shape membership function with CMOS circuit, as shown in Eq. (1). However not more another papers have reported to generate this shape (Azeem et al., 2006; Wei-zhi et al., 2006).

$$\mu(x) = e^{-(x-c)^2/2\sigma^2} \qquad (1)$$

Where c is the mean of the Gaussian curve and σ is the breadth. Fig.5 shows block diagram of digital Gaussian shape generator. It uses two differential amplifiers, two PMOS current mirror, and two reference voltage. In this block diagram all transistors operate in saturation region when vi increase we can obtain Gaussian current I_{o1} .by changing two reference voltage we can change slope of output shape. We apply Flash A/D to this output and we generate digital Gaussian shape. We assume two differential amplifiers have same specification. Mismatch between them make asymmetric shape.

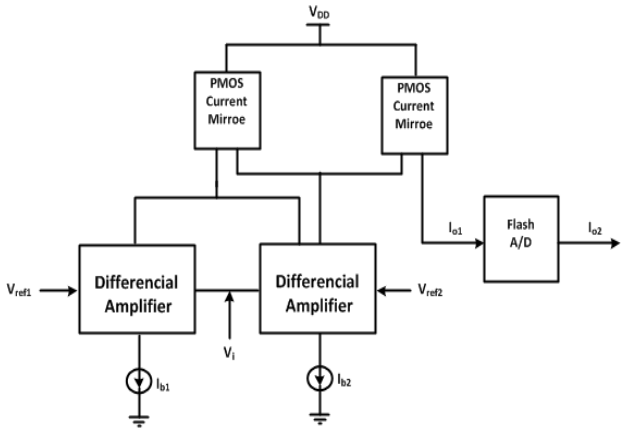

Fig. 5: Block diagram of Gaussian shape with digital output

System simulation

All circuits have been simulated using hspice in 0.35µm CMOS standard technology. For proposed Flash A/D, It should be noted that several simulations have been performed with different input signal frequency varying from a few MHz to 25 MHz. fig.6 (a) shows Input and reference currents in range 16uA, ramped and fixed shapes, respectively. By Appling this input to the proposed Flash A/D we have obtained fig.6 (b) with 4 bit resolution.

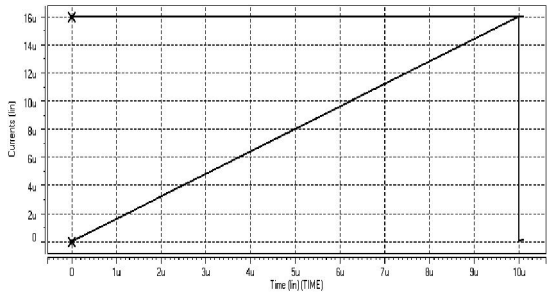

fig.6: Input and reference currents in range 16uA, ramped and fixed shapes, respectively

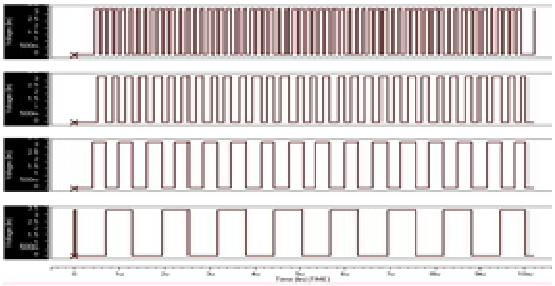

fig.7: output of proposed Flash A/D with 4 bit resolution.

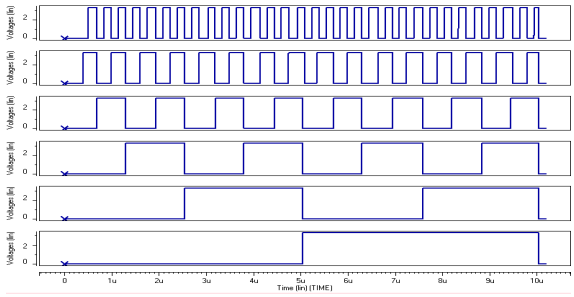

Fig.8: out output of proposed Flash A/D with 6 bit resolution by increasing amplitude of input current.

We can increases resolution of flash A/D up to 6-bit. Fig.8 shows output of circuit with 6-bit resolution. To obtain his figure we have increased amplitude of input current.

After simulation proposed flash A/D, we have used mentioned circuit to obtain trapezoidal with digital output. Fig.9 shows result of simulation of proposed programmable trapezoidal MFG.

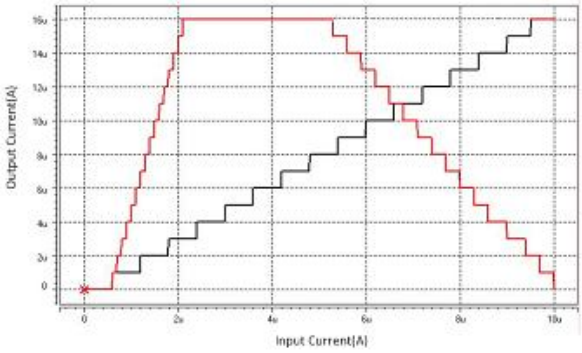

Fig.9: simulation of proposed programmable trapezoidal MFG with 4-bit resolution

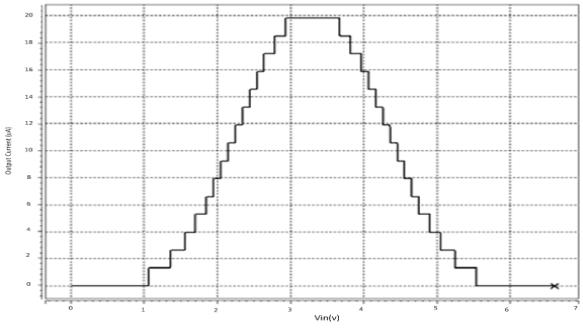

Fig.10: symmetrical Gaussian curve with digital output

The output of Gaussian curve is shown in Fig.10 When symmetrical curves are desired, transistors Size on both differential amplifiers must match. Programmability of the output current shape is obtained by varying the difference between the reference voltages.

Conclusion

Gate-level design of MFC increases its hardware, and pure analog implementation makes it lack of flexibility and programmability. Therefore in this study we have designed analog MFC with digital outputs, which is capable of generating different shapes (triangular, S-shape, Z-shape and trapezoidal). By combining flash A/D and MFC together less hardware is required. Also by appling proposed flash A/D to simple circuit, a programmable Gaussian shape applicable in data classification is obtained. We take advantages of Current-mode circuits such as high speed, low power consumption, large dynamic range, and high flexibility. All circuits are simulated by hspice in 0.35μm CMOS standard technology.

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REFERENCES

Abuelma'ati,M.T. and A. Shwehneh,(2006)," A Reconfigurable Gaussian/Triangular Basis Functions Computation Circuit", Analog Integrated Circuits and Signal Processing, 47, PP:53–64.

Azeem .M. F., and K.P. Govila,(2006)," Design Of Analog CMOS Based Fuzzy Inference System" 2006 IEEE International Conference on Fuzzy Systems, Vancouver, BC, Canada, July 16-21, PP:1715-1720.

Basterretxea .K., J.M. Tarela and I. del Campo,(2006)," Digital Gaussian membership function circuit for neuro-fuzzy hardware", Electronics Letters 5th January Vol. 42 No. 1.

Bouras S, Kotronakis M, Suyama K and Tsividis Y (1998) Mixed analog-digital fuzzy logic controller with continuous-amplitude fuzzy inferences and defuzzification Fuzzy Systems. IEEE Transact. 6(2), 205–215.

Di Cataldo D, Liberali V, Maloberti F and Palumbo G (1996) A/D conversion with fuzzy membership function. In: Proc. EUSIPCO'96, Trieste, Italy. Sep. pp: 1279–1282.

Dualibel, C.; Jespers, P.; Verleysen, M.;(2001)," On designing mixed-signal programmable fuzzy logic controllers as embedded subsystems in standard CMOS technologies", 14th Symposium on. Integrated Circuits and Systems Design PP: 194 – 200.

Gabrielli A., E. Gandolfi, M. Masetti, and M. R. Roch,(1997), "VLSI Design and Realisation of a 4 Input High Speed Fuzzy Processor," 6th IEEE Int. Conf. on Fuzzy Systems, vol. 2,july, pp. 779-785.

Geun Bum Koo; Jin Bae Park; Young Hoon Joo; Hyoung Seok Jeon;(2011)," Digital controller design for fuzzy systems with packet loss: Intelligent digital redesign approach", IEEE international conference on fuzzy systems PP: 1989 – 1993.

Gianluca Giustolisi, Gaetano Palumbo and Salvatore Pennisi (2002) Current-mode A/D fuzzy converter. IEEE Transact. Fuzzy Sys. 10, 533-540.

Gregorian .R., K. W. Martin, and G. C. Temes,(1983), "Switched-capacitor circuit design," in Proc. IEEE, vol. 71, . Aug. PP: 941-966.

Guo, S.; Peters, L.; Surmann, H.;(1996)," Design and application of an analog fuzzy logic controller", IEEE Transactions on fuzzy systems. Volume: 4, PP: 429 – 438.

Jacomet .M. and R. Walti, (1994),"A VLSI Fuzzy Processor with Parallel Rule Execution,' Proc. IEEE Int. Conf. on Fuzzy Systems, PP: 1-5.

Kachare, M.; Jaime Ramirez-Angulo; Carvajal, R.G.; Lopez-Martin, A.J.(2005)," New low-Voltage fully programmable CMOS triangular/trapezoidal function Generator circuit", IEEE Transactions on Circuits and Systems I: Regular Papers, Volume: 52, Oct. PP: 2033 – 2042.

Liviu tigaeru,Dimitrie alexa, Ovidiu Ursaru,(2003)," New Analog Mode Membership function circuit" IEEE International Symposium on Signals, Circuits and Systems, SCS 2003,PP: 601-604.

Madrenas .J., M. Verleysen, P. Thissen, and J. L. Voz, (1996)," A CMOS Analog Circuit for Gaussian Functions", IEEE Transactions on Circuits and Systems-II: Analog and digital signal processing.VOL.43,No. I, Jan, PP:70-74.

Mohammad Ababneh, Ahmed Muhammed Almanasreh, Hani Amasha,(2009)," Design of digital controllers for uncertain chaotic systems using fuzzy logic", Journal of the Franklin Institute, Volume 346, Issue 6, August, PP: 543-556.

Patyra, M.J.; Grantner, J.L.; Koster, K.;(1996)" Digital fuzzy logic controller: design and implementation", IEEE Transactions on fuzzy systems.Volume: 4, PP: 439 – 459.

Roberts .G. W. and A. S. Sedra,(1991) "Synthesizing switched-current filters by transposing the SFG of switched-capacitor filter circuits," IEEE Trans. Circuits Syst., vol. 38, pp. 337-340, Mar. 1991. Circuirs Syst., vol. 38, PP: 337-340.

Tokmakci ,M., M.Alci and R.Kili,(2002)" A Simple CMOS-Based Membership Function Circuit", Analog Integrated Circuits and Signal Processing, 32, PP:83–88.

[2] Vidal-Verdu, F.; Navas, R.; Rodriguez-Vazquez, A.(1997)," A modular CMOS analog fuzzy controller", Proceedings of the Sixth IEEE International Conference on fuzzy systems, Volume: 2, PP: 647 - 652.

Vidal-Verdu, F.; Navas-Gonzalez, R.; Rodriguez-Vazquez, A.;(1998)," A mixed-signal fuzzy controller architecture", 1998 IEEE International Conference on Electronics, Circuits and Systems, Volume: 1, PP: 423 – 426.

Weiwei Shan; Yuan Ma; Newcomb, R.W.; Dongming Jin;(2008)," Analog Circuit Implementation of a Variable Universe Adaptive Fuzzy Logic Controller", Express Briefs, IEEE Transactions on Circuits and Systems II, Volume: 55, PP: 976 - 980 .

Wei-zhi Wang, Dong-ming Jin,(2006)" Neuro-fuzzy system with high-speed low-power analog blocks", Fuzzy Sets and Systems, Volume 157, Issue 22, 16 November, PP: 2974-2982.

Yamakawa .T., (2011)," Electronic circuits dedicated to fuzzy logic controller", Scientia Iranica, Volume 18, Issue 3, June, PP: 528-538.