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Hardware Implementation of an Adaptive Mixed Signal Neuro Fuzzy System Using High Speed and Low Power Analog CMOS Circuits

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ABSTRACT

In this paper we design of an adaptive Nero fuzzy system with mixed-signal inputs and digital outputs. In this paper analog advantages including low die area, high speed and simplicity are added to the digital advantages, such as programmability, robust against noise and distortions. a new programmable Fuzzifier circuit based on mixed-signal input, and min circuit for inference and Multiplier/Divider circuit for defuzzifier block and a current mode high speed flash Analog to Digital (A/D) converter with 4bit resolution are proposed. The inference speed of the system is about 18.18 MFLIPS. The controller simulated in 0.35um CMOS standard technology.

KEY WORDS: fuzzy controller,current-Mode,fuzzification,Mixed signal, flash A/D.

INTRODUCTION

The application of neuro-fuzzy technologies to real-time control problems demands the development of new processing structures which allow efficient hardware implementations of fuzzy inference mechanisms.

Recently, the combination of neural networks and fuzzy logic has received attention. The idea is to lose the disadvantages of the two and gain the advantages of both. Neural networks bring into this union the ability to learn. Fuzzy logic brings into this union a model of the system based on membership functions and a rule base. Real-time control of non-linear plants is often a hard and computationally intensive task. Neural networks and fuzzy systems (neuro-fuzzy systems, in general) are raising more and more interest in the field of real-time control thanks to their superior performance. Advantages of neuro-fuzzy techniques are their non-linear characteristics, the capability of learning from examples, the adaptation capability, etc.

Furthermore the availability of dedicated neuro-fuzzy processors permits a very fast implementation of neuro-fuzzy algorithms, and therefore it allows to use these methods in real-time applications, where a quite high sampling rate (namely, >1kHz) is required. Fuzzy logic controllers are available implemented on two options: the software (Cabrera Et.al, 2004), (Iluminada et.al ,2000) and the hardware approaches. Software-based fuzzy controllers are limited to a slow-speed operation and so they are not efficient for real-time applications. In software solution, a simple program can be written to emulate the system so that the input values are subjected to rules that are predefined per the system's requirements. Once passed through the rules of the system, the output can be determined and translated into an order to execute the appropriate function. This process involves three stages: the fuzzification of the inputs, the fuzzy inference process, and the defuzzification of the output. Fuzzification implies the change from distinct inputs into interpreted sets through an analysis of how close in membership each input is to those predefined sets. Fuzzy inference is where the fuzzy values from the fuzzification process are compared to each predefined rule in order to determine the proper fuzzy output value. Defuzzification implies the translation of the fuzzy output into a distinct value through a simple calculation involving the output membership set values and conversion factors. All of this can be done within a software program with set functions to calculate and process each stage. Therefore, each software application can be customized to suit the system's needs specifically, making this solution process very flexible. However, since this is software based, reading in of inputs, writing out of outputs, and all the internal calculations done within the software call for extra time per calculation that can limit a process that may require faster calculations. In addition, as it is software, it is limited to use on the computer. A way to help get around this is to implement the software into Microcontroller circuits. This speeds up the process a little bit and makes the software portable so that it can be used in individually designed circuits like basic control systems. Again, this is not as fast as it could be which is still a limiting factor and plays a role in systems that require very quick response times. The demand for high-speed execution of the fuzzy inference made the hardware approach becomes attractive. Many systems require very quick calculations, including many physics experiments where time is of the essence. Hence a hardware solution is best. Depending on the design technique employed, fuzzy hardware is classified into three groups: analog (Peyravi et.al ,2002),(Dinavari et.al, 2009),(Guo et.al,2009) digital (Patyra et.al,1996),(Sánchez et.al.1997),(Aminifar el.al,2006) or mixed-signals (Amirkhanzadeh el.al,2005), (Yosefi et.al,2011),(Gianluca et.al,2002) and(Baturone et.al ,2000)which combined analog and digital signals for processing the information.

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This work is based on hardware implementation of a fuzzy controller which analog advantages such as low die area, high speed and simplicity are added to the system advantages, whose output is digital considering unchanged digital system properties. Hence, we proposed the new CMOS integrated circuits to implement fuzzy controller chip with mixed-signal input and digital output, while the internal blocks (Fuzzifier, Inference and Defuzzifier) are realized by current-mode analog circuits. The advantages of current-mode approach are a great and flexible range of value and high speed.

LITERATURE REVIEW

During the last decade a growing interest in low voltage low power circuit in standard CMOS technology can be observed because of portable electronic devices and the smart sensors. Current-mode circuit shows great future since using current as signal carriers enables it to be unrestricted by supply voltage. A fully current-mode mixed signal fuzzy controller will meet the demand as mentioned above. Previous approaches to use of analog circuits for fuzzy controller did not actually present methodologies for monolithic design, but rather focused on the realization of different technologies (Wilamowski &jaeger, 1999), (Aboushady et.al , 2002).Also they covered mainly the case where the input-output function of controller remains fixed, not appropriate for most practical applications, where the exact function is unknown a priori or must adapt to specific environmental characteristically. For this reason many analog hardware implementations of fuzzy engines are reported in the many literatures. The current-mode fuzzy engine proposed in (Sasaki et.al, 1992) implements the normalization condition using a feedback loop, which forces the input membership functions to realize a partition. In research of Kettner et,al (1993) some Membership Function Circuits (MFCs), with a piecewise linear characteristic, are proposed. Similarly, Huertas et,al (1996) proposes a triangular/trapezoidal MFC. However the main lack of those approaches is that the output of the fuzzy system is non-smooth. A tunable voltage-driven MFC has been proposed in Chen et.al (1992) paper, implemented using a source-degenerated differential pair, and in Franchi et.al (1998) research a similar MFC is coupled with a custom inference engine. Likewise, Rodr´ıguez et.al (1999) presents some fuzzy engines with differential-pair based MFCs, adopting the min-max inference method, with either normalization based or division based defuzzyfication.

ANN STRUCTURE

A. Artificial Neural Network (ANN):

For analyzing ANFIS architecture let us consider the summery of ANNs structure. They are computing systems based on an analogy with the work of the nervous system of the brain, in which connections organize neurons into the networks. Therefore they are combination of mathematical functions considering neurons. Because of neuron interconnections and using kind of mathematical functions, there are different structures for various applications, in which feed forward ANNs are much more usual than another ways. The ANNs learns from samples of input-output data that the used learning algorithm is based on multilayer error-correction learning, also called back propagation. This learning procedure is also called training. There are two types of training algorithms: “online” training where neural network parameters are updated after each sample presentation, and “offline” training where neural network parameters are updated after all samples are presented. In this work, the “on-line” training approach is chosen for ANFIS since it is more efficient in most cases.

B.ANFIS Architecture

Functionally the ANFIS architecture is the major training routine equivalent to Tkaki-Sugeno first order fuzzy inference systems (FIS). ANFIS uses a hybrid learning algorithm to identify parameters of Sugeno-type FIS. It applies a combination of the least-squares method and the back propagation gradient descent method for training FIS membership function parameters, to emulate a given training data set. In other words to start ANFIS learning, first a training data set is required that contains desired input/output data pairs of the target system to be modeled. The ANFIS structure used to implement fuzzy controller with five layers is shown in Figure 1. It consists of two inputs, four membership functions for each input, sixteen fuzzy rules and one output. The ANFIS applies fuzzy inference techniques to data modeling. According to this structure, the shape of the membership functions depends on parameters, so changing these parameters will change the shape of the membership functions. The benefit of this method is that it chooses the membership function parameters automatically, that’s better than just monitoring the data and estimates these parameters.

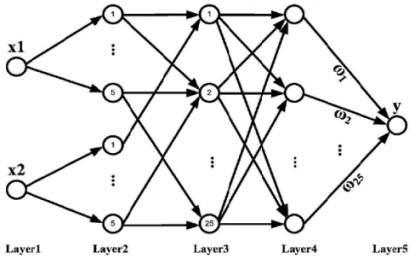

Fig 1 : ANFIS architecture of fuzzy controller model.

Circuit Design Strategies

A. CMOS Membership Function Circuit (Layer 1, 2):

Membership function circuit (MFC), whose transfer characteristics represent the ant cedents' membership functions. They provide the degree of matching between the controller input signals andthe antecedents of the rules.

The main new integrated circuit to implement MFC block is shown in Fig. 3. According to the differential pair (M1 and M2) and using a simple MOS transistor model for strong inversion, the current output for membership functions in the end of input range are given by Wilamowski et.al (1999)

$$I_i = \frac{1}{2} I_o \times$$

$$[1 + (V_{in} - V_{REFi}) \sqrt{(\frac{\kappa}{I_o}) - (\frac{\kappa}{2I_o})^2 (V_{in} - V_{REFi})^2}]$$

Where I_O is the normalized current source, $\kappa = \mu CoxWi/Li$, V_{in} is the input crisp voltage and V_{REFi} are the reference voltages. In the point of ($V_{in} = V_{REFi}$), two currents of Ii and Ii+1 are same and equal to the half of IO. The maximum of (Vin - VREF) is extracted by deriving it to the Ii and then resulted $\sqrt{2}\Delta V0$. In other words the voltage of $\sqrt{2}\Delta V0 = \Delta V1$ is needed to that transistor enter to the cutoff and leaner regions respectively. Because of adding another transistor and being in saturation region, according equation the least voltage of $2\sqrt{2}\Delta V0$ between V_{REF1} and V_{REF2} is needed to have being I_1 and I_2 in minimum and maximum current quantity respectively.

$$V_{REF2} = V_T + \Delta V_1 - V_T + V_{in} = \Delta V_1 + V_{REF1} + \Delta V_1$$

$$= 2\Delta V_1 + V_{REF1} \Rightarrow V_{REF2} - V_{REF1} = 2\sqrt{2}\Delta V$$

With these results, the proposed fuzzifier circuit (Fig. 2) has capable of obtaining Gaussian membership function shapes (I1 to In) with tuning voltage references in least quantity (VREF2-VREF1=$2\sqrt{2}\Delta V0$). Increasing different voltage references and distancing the equality points from each other, cause to have Trapezoidal shapes. Choosing different transistors sizes in 1, 2, 4 and 8 ratios, and by acting binary control switches, the suitable changing slopes can be accomplished. Setting different voltage references in least quantity and using high control switches, the introducing Triangular membership functions are resulted. Even though the proposed circuit is very simple and flexible, equally spaced symmetrical membership functions were chosen in VLSI implementations and has capable of introducing three different shape types without any complexity and using extra hardware in contrast before works (Bouras et.al,1998), (Sasaki et.al , 1992),Kettner et,al (1993, Franchi et.al(1998)

B.Min Operator (layer3):

Our used connective for compounding antecedents is "AND" operator which implemented using improved Min circuit from (Patyra et.al,1996),(Yosefi et.al,2011), (Saavedra et.al, 1999). The output of a fuzzy inference engine is a fuzzy set which represents the possible distribution of control action. Among the suggested defuzzification strategy, the Center of Area (COA) method is used here (in this case, because of singleton output membership function, it is called weighted average of singleton) for defuzzification

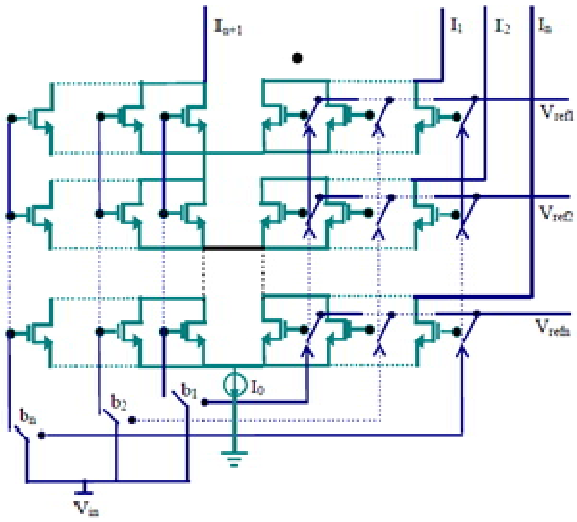

Fig. 2: Membership function Generator with Mixed-Signal

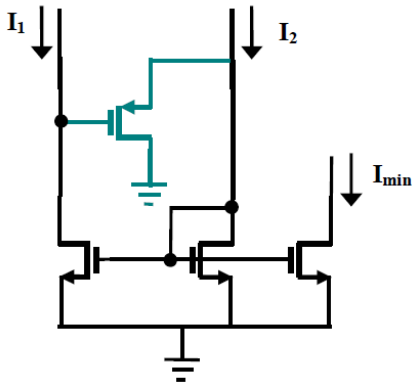

Fig. 3: Minimum Circuit

C. Multiplier/Divider Circuit (layer4,5):

The principle of operation of the multiplier is based on the square-difference identity :(Naderi et.al, 2009)

$(X + Y)^2 - (X - Y)^2 = 4XY$

The analog multiplier circuit is shown in Fig. 4. It is based on the squaring circuit and two dual translinear loops.The first loop (M1.M4) provides a(X+Y) input function to the squarer function $(X + Y)^2$ and the second loop(M5.M8) provides a $(X - Y)$ input function to the squarer function $(X - Y)^2$

$$I_{O1} = \frac{(I_X + I_Y)^2}{4I_B} + I_B$$

$$I_{O2} = \frac{(I_X - I_Y)^2}{4I_B} + I_B$$

$I_0=I_{O1}-I_{O2}$

Substituting two before equations into last equation results in

$$I_{out} = \frac{I_X I_Y}{I_B}$$

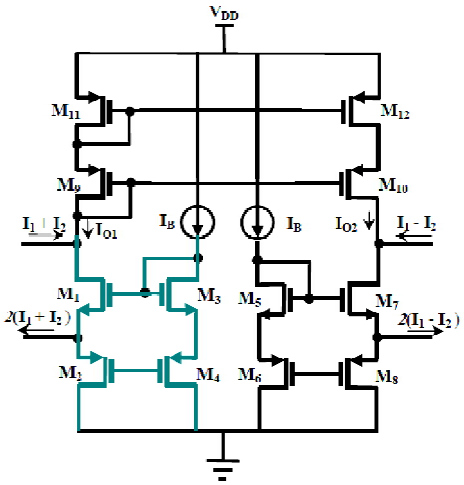

Fig. 4: Multiplier Circuit

D . Current-Mode Flash A/D :

Recently, current-mode comparators have been used to implement analog to digital converters [15: (Aboushady et. al, 2002), 23: (Bell et.al, 2001)]. In this paper, we propose architecture for 4 bit FLASH A/D converters based on a current-mode comparator. Figure. 5 shows the general architecture of an N-bit Current-mode FLASH A/D.

Converter. It is composed of 2^N current-mode comparators.

The input signal (Iin) is copied and distributed to all the comparators using identical PMOS current mirrors. A reference input current is also necessary which determines the ADC input range. The reference signal (Iref) is divided to 2^N pairs of NMOS and before distributed to all the comparators gradually increases (I1, I2…I16) using identical current mirrors.

Figure. 6, shows the current-mode comparator circuit. It is made up of NMOS and PMOS transistors and two inverters. at input of this converter (node C), Iin is compared to Iref , If Iin > Iref the voltage of node c increases and last output of two inverters shows "1" logic, otherwise it switches to "o" logic. The output of inverter is known as thermometer and should convert to binary.

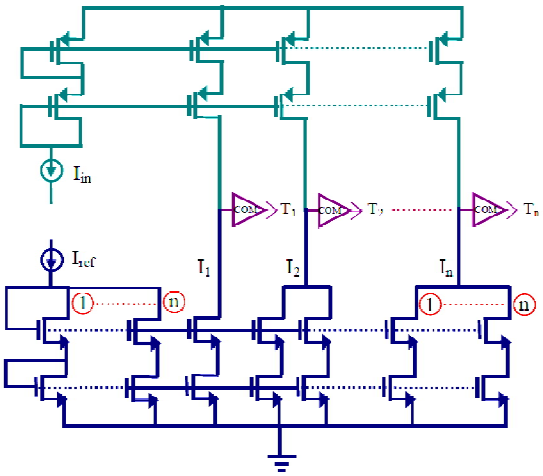

Fig. 5 : Current-Mode Flash A/D

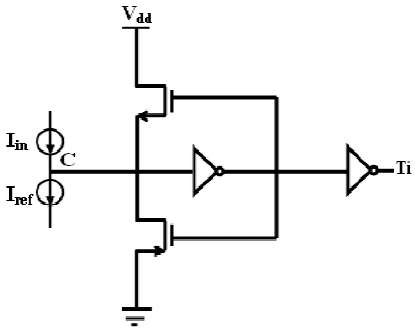

Fig. 6: Current-Mode Comparator

System Simulations :

The proposed chip architecture designed and implemented using Hspice software. Implementation will be based on the specifications obtained from the modeling.

Depending on simulation data the structure optimized for High reconfigurability and controllability, improved scalability and sampling. However to achieve best performance, Implementation and analysis of the implemented parts with FPGA will be practiced in real conditions.

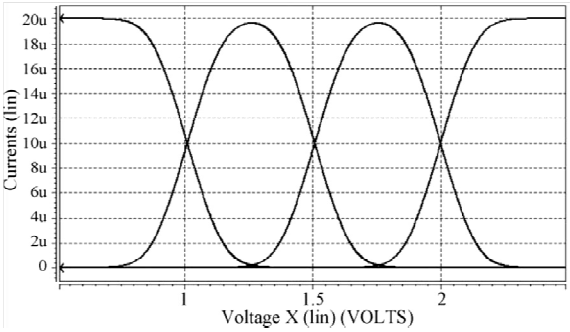

Fig. 7: Gaussian Membership Functions obtained from fuzzifier circuit

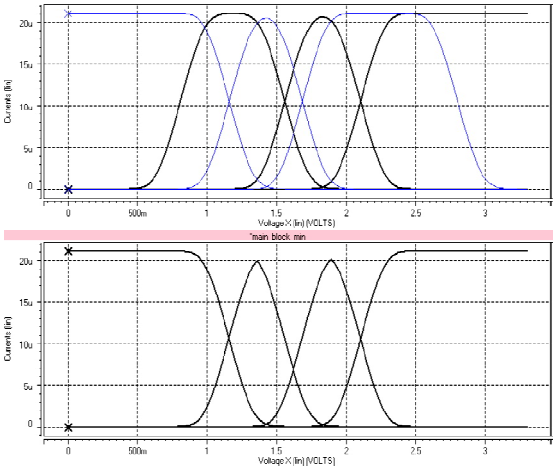

Fig.8.applying fuzzifier to the minimum circuit

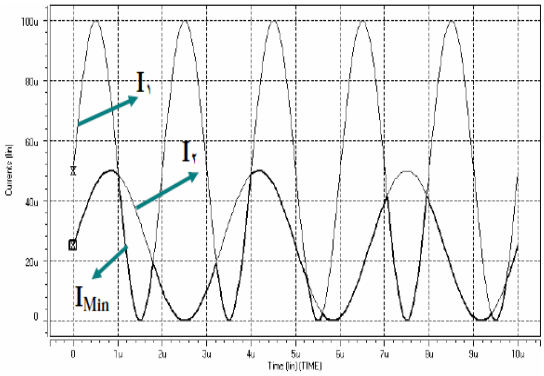

Fig.9. Simulation of minimum circuit

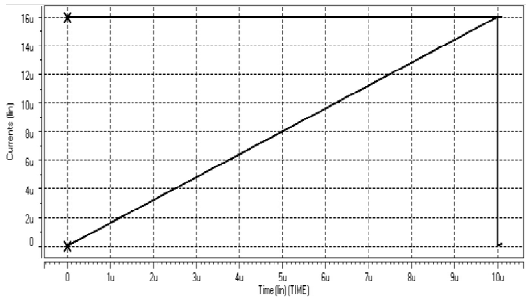

Fig.10. Input and reference currents in range 16uA, ramped and fixed shapes, respectively

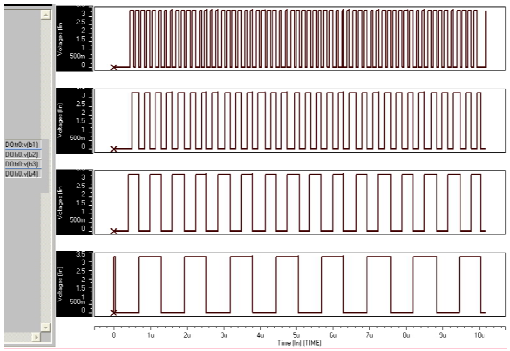

Fig.11. Simulation results of 4 bit Flash Current-Mode A/D

CONCLUSION :

The proposed FLC chip with mixed-signal input and digital output is provided by internal analog part advantages while the digital output supports microcontroller and microprocessor environments. This controller including new and improved integrated CMOS circuit of Fuzzifier, Min operator, Multiplier/Divider, and current-Modea Flash A/D simulated in 0.35um CMOS standard technology. Simulation results show that with power consumption of 13.5 mw, its inference speed reaches 18.18 MFILPS.

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