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Analysis and Simulate CMOS circuit by using fuzzy logic

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ABSTRACT

In this research, we try to present a new method for analyzing and simulating the electronic circuits. Among electronic circuits, as CMOS circuits have a wide usage in various basis of industry, our focus is on such circuits. The specification of this new method, is the way which we use to analysis and simulate circuits. In software, designing by this method, instead of using classic mathematics, we use fuzzy logic. The advantage of using fuzzy logic, is improving rapidity and delicacy of simulation. In this method, the basic elements are fuzzy interfaces. So, by increasing delicacy of these fuzzy interface systems, we can gain the desirable delicacy. So by using fuzzy logic, we can reach a desirable rapidity and delicacy in designed software.

KEYWORDS: Cmos circuit**, F**uzzy logic**, E**lectronic circuits

1. INTRODUCTION

Nowadays, human being's life has an undeniable dependency to electronic and digital instruments. This dependency has propagated in various bases. So optimization of different stage of manufacturing of these electronic and digital segments is very important. Designing section is one of the basic stages of manufacturing. So improve the method of designing, can be very effective for this optimization. Software has a great role in designing and analyzing of electronic and digital segments. During these years, different kinds of software, has been represented and each, has their own benefits and problems and use a special method for simulation. This research is going to introduce a new method of simulating too. The egregious point of this method is the way of implementing calculations. In other methods, whole calculations, needed for obtaining final result, is done by classic mathematics and by ordaining demanded equation which take a long time to be solved. This solving time, may decrease the rapidity of simulation. By replacing fuzzy logic, we have no demanded equation and the time which spends for implementing computation will be omitted. In this method, we use fuzzy interfaces. Instead of each gate in a circuit, we replace a fuzzy interface system. (FIS) These fuzzy interface systems are formed on bases of knowledge. And in this way we improve the rapidity of our method. The other important point is the delicacy of this technique. As, FIS is the base of this method by improving the delicacy of each FIS we can reach to desirable point.

2. Elaboration of method

As mentioned before, in this research, the final aim is introducing a new method for simulating CMOS circuit at gate level, by using fuzzy logic. At first, for each primitive gates, (And, NANDOr, nor and not), an appropriate fuzzy interface system should be built. Afterwards, for simulating circuit, each gate will be replaced by these system. Manufacturing fuzzy systems has different stages but first an explanation about FIS can be useful.

2.1. Fuzzy interface system

Fuzzy inference is the process of formulating the mapping from a given input to an output sing fuzzy logic. The mapping then provides a basis from which decisions can be made, or patterns Discerned. The basic idea of these neuro-adaptive learning techniques is very simple. These techniques provide method for the fuzzy modeling procedure to learn information about a data set, in order to compute the membership function parameters that best allow the associated fuzzy inference system to track the given input/output data. This learning method works similarly to that of neural networks. In other words, this method, by mapping inputs, through input membership functions and associated parameters, and then through output membership functions and associated parameters to outputs, can be used to interpret the input/output map. The process of fuzzy inference involves membership functions, fuzzy logic operators, and if-then rules. There are two types of fuzzy inference systems that can be implemented: MAMDANI –type and SUGNO-type. In this research we use SUGNO -type. There is different type of MFs. Tentatively, TRAPMF type is used in this article. Figure number 1 shows a TRAPMF membership function.

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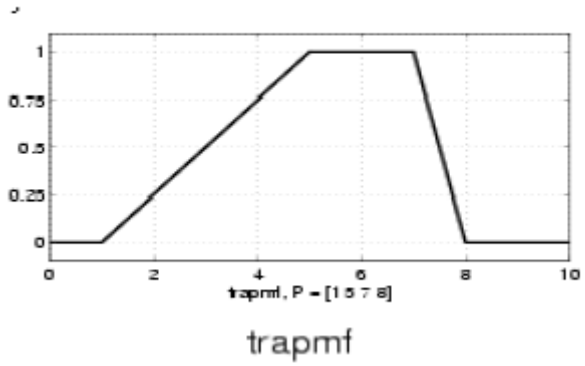

Figure 1: TRAPMF model

The first step is to specify membership function and its parameters. This step is done through training data.

2.2. Obtaining data and train interfaces

The first step is training. This training will result suitable membership functions for fuzzy interfaces. For training these interfaces, perfect and true sets of data is needed. For gaining these sets of data, Spice simulator has been used. Each primitive gate has been simulated in Spice. Different inputs was given to each gate and its output was saved. Each set of data is a text file which includes more than10000 couple of input-output points. These sets construct our knowledge bases. By use of these knowledge bases, we can train data and gain suitable membership functions.

Figure 2 show the membership function for one of the input of an Or gate.

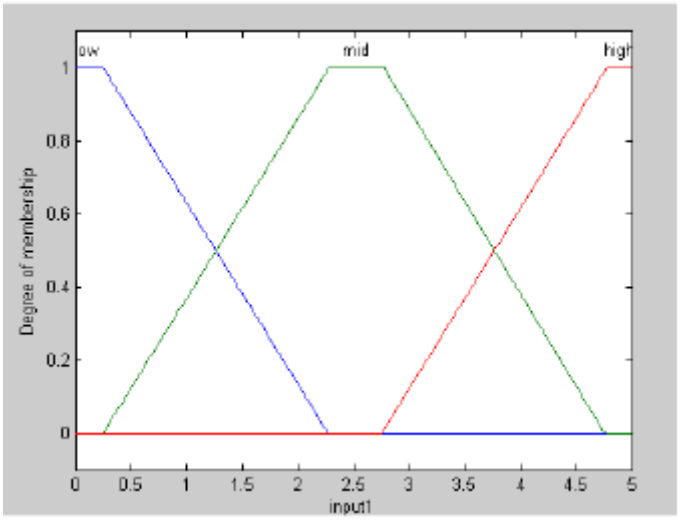

Figure 2 membership function for or gate

As shown in figure 2, the type of MFs are TRAPMF but the important point is to specify the range of each input set. First input and output variable should be specified.

2.3. Input and output variable:

Each fuzzy interface system, (except not) has two inputs and one output. Not have one input and one output. The next step is separating sets. But the range of this separation is different for input and output variables. Each of the input and output variables can get one of these three deals: High, Medium and Low. Finding **the** exact boundary of these three **values** is very important for improving the delicacy of built FIS. According to the logic level of CMOS circuits, we find **these boundaries** as followed:

For input variables:

LOW : 0 – 1

MID : 1–2.1

HIGH : 2.1–5

And for output variables:

LOW : 0 – 2.1

MID : 2.1–3

HIGH : 3–5

Pay attention, the high voltage can be in the range of 0 – 15 in CMOS technology and for this research, 5V is consider as High level.

2.4. Deduction rules

These if-then rule statements are used to formulate the conditional statements that comprise fuzzy logic. After separation the input and output region, we can form this rules. According to data sets, gain from Spice and boundary of separation these rules is obtained. For an Or gate, some of these rules when the first input is low or med are represented as followed:

IF X1 IS LOW AND X2 IS LOW THEN OUT IS LOW

IF X1 IS LOW AND X2 IS MED THEN OUT IS MED

IF X1 IS LOW AND X2 IS HIGH THEN OUT IS HIGH

IF X1 IS MED AND X2 IS LOW THEN OUT IS MED

IF X1 IS MED AND X2 IS MED THEN OUT IS MED

IF X1 IS MED AND X2 IS HIGH THEN OUT IS MED

These rules are very important .Optimizing these rules may have a great effect on optimization of the whole system.

3. Final FIS

After following all the mentioned steps, process of building a fuzzy interface system is completed. From now on, in a digital circuit, instead of each gate, a fuzzy interface system is called and this replacing increases the rapidity of simulation process. Figure 3 shows a three dimension schema of the output of a fuzzy interface system, written for an Or gate.

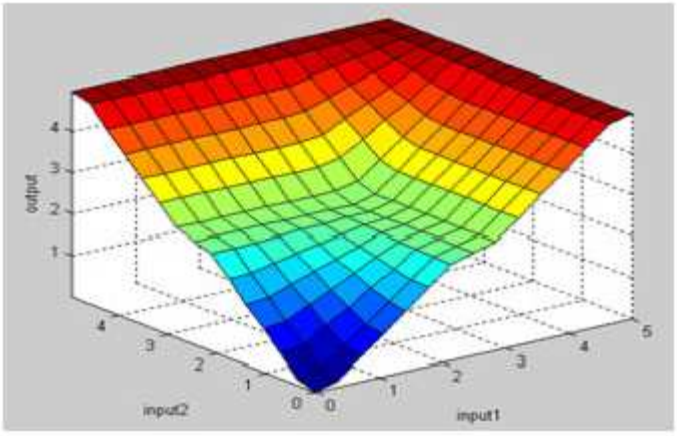

Figure 3: ORFIS output

In this figure, the output resulted by two input is shown. The effect of written rules and boundary voltages is obvious in the figure. From the point of view of delicacy, by optimizing deduction rules, membership function and logic operators, the desirable delicacy have been obtained. On the other hands, by increasing the number of input-output couples, in data sets, we can improve the delicacy but pay attention that the number of these couples should be limited. Because after a special point, if the number of training data increases, the system begins over fitting and acts vice versa and delicacy decrease. Figure 4 shows the fault of a fuzzy interface system written for a NAND gate.

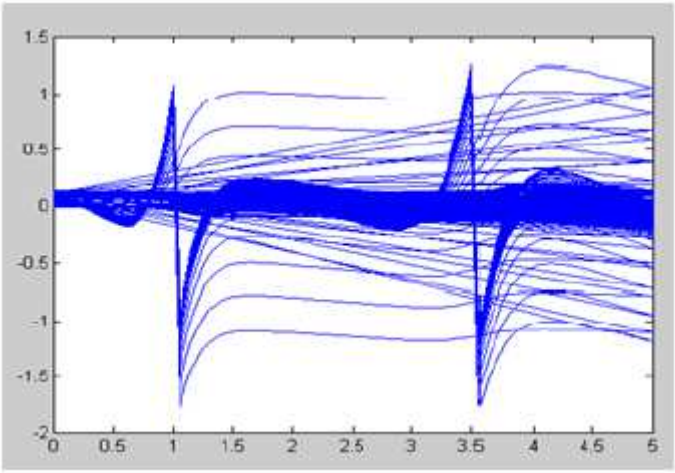

Figure 4.fault in a NAND FIS

As shown in figure 4, except a few critical points, the fault is less than 0.12 and this fault is ignorable**.**

4. FIS function

After building the whole set of FIS, (for all of the primitive gates) it is time to examine the function of designed FIS. For gaining this aim, as an instance, a circuit is selected. This selected map is a 16 bit comparer. Once the map was simulated in Spice and gets the outputs. Then FIS structures were called to simulate the circuit and get the outputs. This circuit has three outputs: The first shows the output for the state of A = B. when A is the first input and B is the second input. The second, shows the output for the state of A< B and the last, shows the **output for the state of A > B.** These three outputs has been gained from both Spice and FIS simulator and the**ir results was compared together**. The outputs for both simulators are evaluated for the same couples of inputs. In figure 5 one of the outputs of FIS simulator is shown. This is the output of state of A > B.

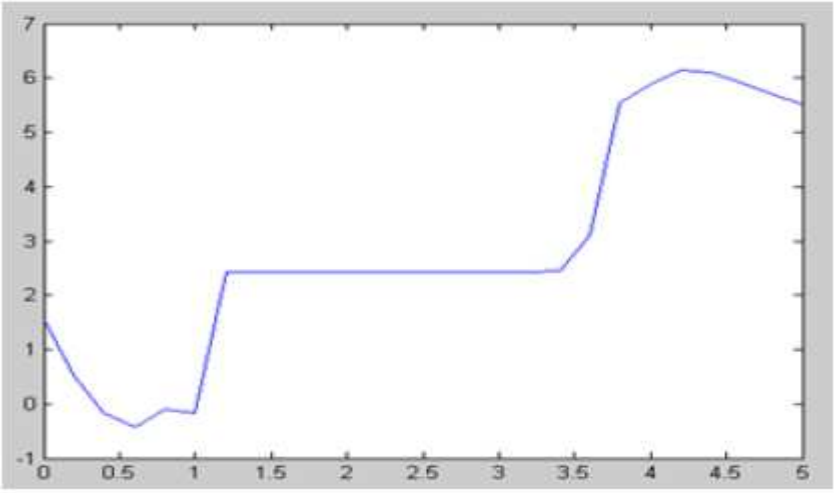

Figure 5. A > B

By comparing the result of two simulators, this result is obtained: the error of the fuzzy simulator is about 0.12. The second output is shown in figure 6.This is the output of state of A < B.

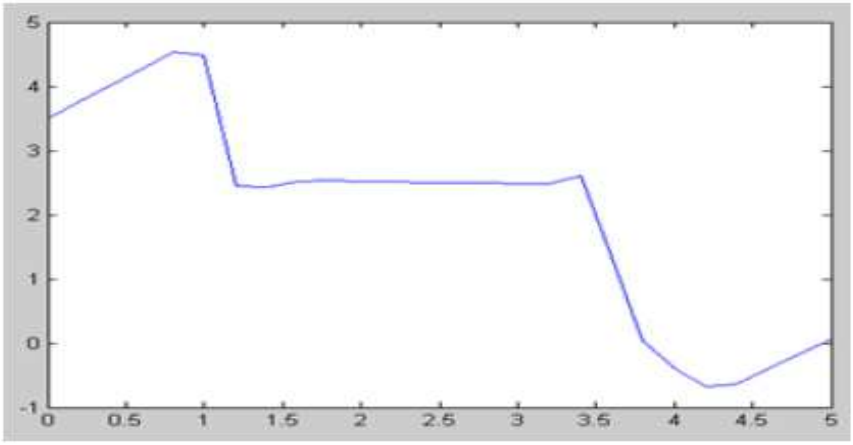

Figure 6. A< B

The time which took by each of the simulators was calculated. This time calculation, show how much efficient **is using** fuzzy system**.**

Table 1: improvement of simulation time

	Fuzzy Sim	Spice
Xor gate	0.54	10.24
BCD to access-3	31.0	186.2
2-bit comparer	39.7	247.3
4-bit comparer	83.4	481.8

5. Conclusion

Using this new method can decrease the time of simulating and increasing the delicacy. The fault of this method is about 0.12. Table number 1 shows the improvement of simulation time by using fuzzy logic.

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