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Architecture for Range, Doppler and Direction finding Radar

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ABSTRACT

Radar signal processing is a well-established field. Accurate and efficient information extraction related to target is main goal of a radar designer. As it has applications in many areas, different architectures have been proposed for its signal processor. Radar capable of localizing a target can be used with missile launcher to hit the target. A radar signal processor with range, Doppler and direction of arrival estimation is presented with its architecture on FPGA.

KEYWORDS*:* Radar; Target; FPGA; Correlation; Doppler; Direction of arrival.

1. INTRODUCTION

Radars can be used for ground and air surveillance. History of Radar lies back to world-war II [1]. A pulse Doppler radar is capable of finding range, Doppler and direction of a target. Architectures of Radar signal processors are given in [2] specifically for Automotive applications is given in [3]. Pulse Doppler radar transmits pulses and the reflected Echoes are processed to target's information. The reflected pulses return to the Radar antenna, which are processed using FPGA, DSP etc. to obtain required parameters. In this paper, we have discussed Radar signal processor of a Pulse Doppler radar capable of finding range, Doppler and direction. Method for finding direction of arrival using 2x2 Array is discussed with its embedded architecture. Design methods and FPGA block diagram discussed are helpful for a Radar designer.

The organization of this paper is now presented. Section II in this paper discusses the algorithm used for finding range and Doppler of target. Section III gives the design methodology of the Radar signal processor and details of FPGA are shown in that section. Estimation of direction of arrival using array is presented in section VII. Finally section VII concludes the paper.

2. Algorithm for Range/Doppler Processing. Radar Antenna transmits pulses with a PRF of 600 Hz, each PRI is 3ms long with 20 % duty cycle. The received pulses after reflection are stacked in a matrix. There are 2^{14} samples in one PRI (3 ms) after A/D. Fig. 1 shows the stacked pulses for 2 targets.

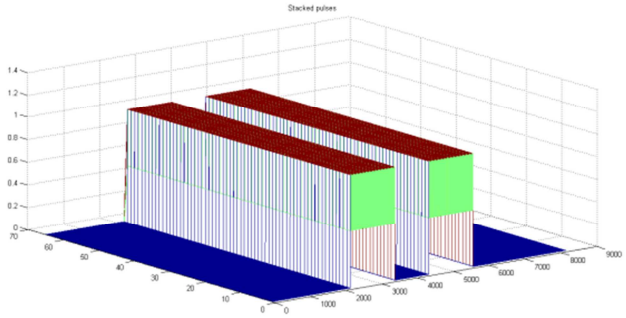

Figure1. Stacked pulses

The Matrix is then passed through column wise FFT which gives Doppler axis [4]. After which correlation is performed row wise which results in range axis. Correlation is performed by using the fast correlation procedure [5]. After correlation of the rows, peaks are obtained corresponding to targets. The primary axis represents range and secondary axis represents Doppler. Thresholding gives much smoother peaks. The summary of algorithm[4] is shown below in Fig. 2

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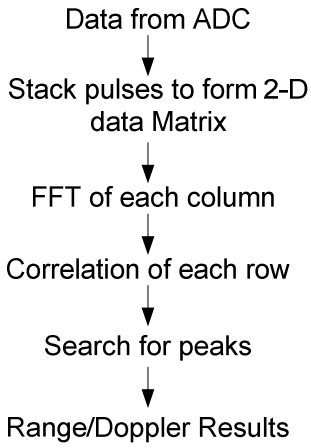


Figure 2. Algorithm Flow Diagram

Hardware/Software Partition. For Hardware implementation there are some control blocks and some processing blocks, so the whole system has to be divided into 2 parts i.e. software and hardware partitions [6]. Design partitioning and verification methodology are crucial steps for the designer for hardware/software co-design. Verification of software based design is easy but verification of VLSI based designs is challenging. The proposed hardware/software partition is shown in Fig. 3. The coprocessor functions and the memory read/write are all performed in hardware part. Decisions such as to check if the required number of samples is available at the FFT/IFFT stage are performed in the software partition. Similarly checks of data available at output of FFT, which next stage is to be applied, all are performed in software partition. The received pulses are stored in DDR with ($256x2^{14}$)locations.

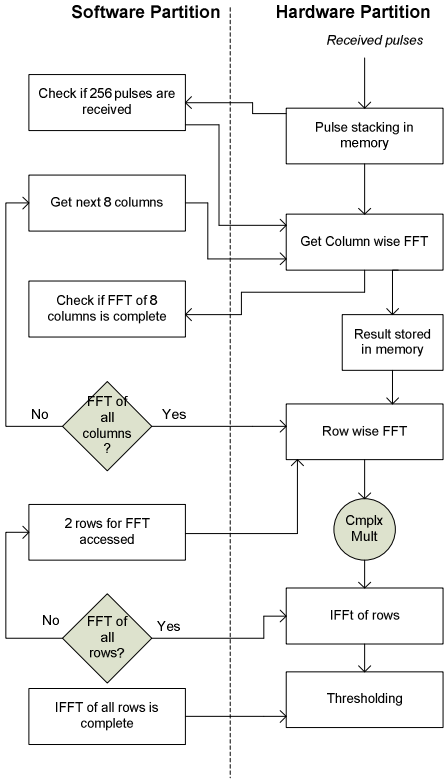


Figure 3. Hardware/Software Partition

The FPGA block diagram and coprocessor details are shown in Fig. 4. The control unit has finite state machines (FSM) which ensures that flow of different signals is correct between different blocks.

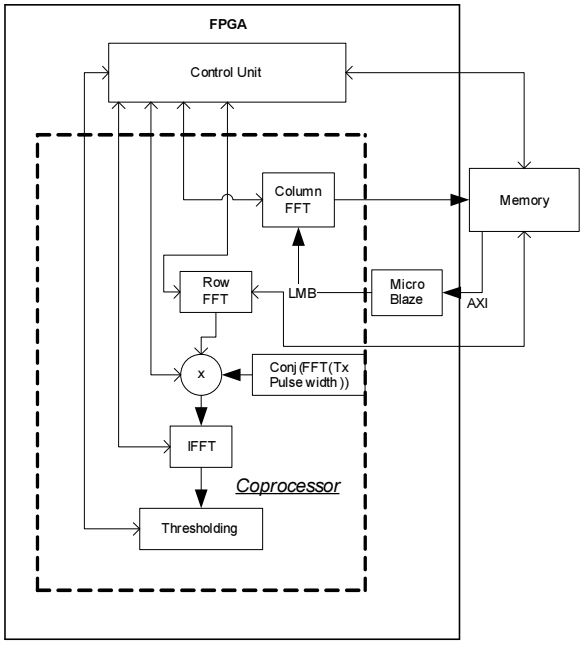


Figure4. FPGA block diagram

We have used Digilent Spartan-6 FPGA[7] kit to verify our algorithm on hardware which is shown in Fig. 5

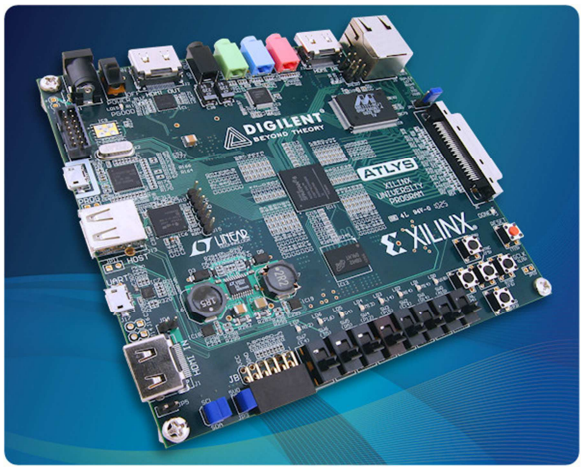


Figure 5. Spartan-6 kit for Implementation

For column FFT, IPcore [8] is used which has many control signals. Some are input signals while some are output signals. The FFT core has to check whether the sequence is available at the input. Correlation is carried out after FFT of the columns. FFT core is used with multiple channels. Buffer RAMS (each has capability to store 512 words) are also used for data storage. The data just after row FFT is sent to complex multiplier. The multiplicand is stored in another Buffer RAM which is offline calculated. Then IFFT core is used so that finally correlation can be obtained. The FFT/IFFT core has an output signal of data valid which indicates that result is now available after processing. The detected targets after processing on FPGA are shown in Fig. 6

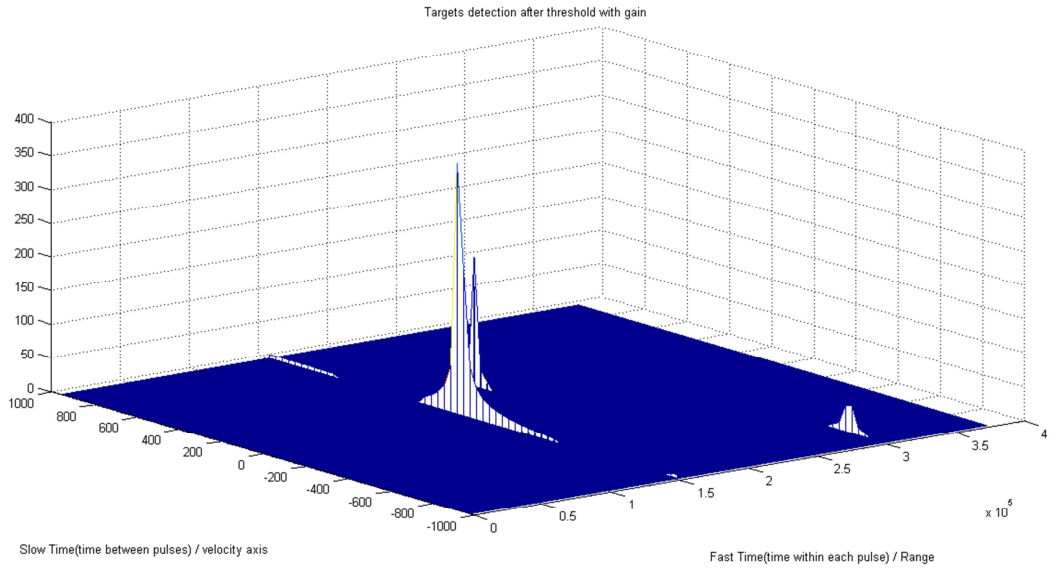


Figure 6. Peaks showing targets detected with range/Doppler information

3. Algorithm for Direction Finding along with Architecture. Estimating the direction of arrival of a target is also in important part of Radar signal processing [9]. Multiple antennas are helpful when using phase difference for estimation of direction of a target. For direction finding, an array of 2x2 antennas is used. The array is shown in Fig. 7

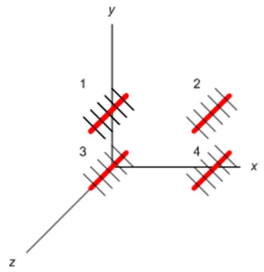


Figure 7. Antenna Array

The phase difference between 2 antennas can be used to find the direction of a target [10]. Fig. 8 shows phase difference between 2 antennas

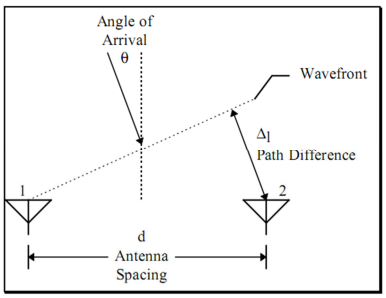


Figure 8. Phase difference in arrival

The path difference ΔI is given by $\Delta I = d \sin\theta$ .The path difference results in a phase difference $\Delta\phi$ between the signals from the two antennas. The relation is given below in Eq. 1

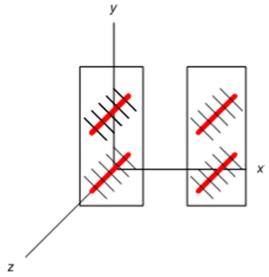
$$\Delta\phi = 2\pi\Delta I / \lambda$$

$$\Delta\phi = 2\pi d \sin\theta / \lambda \qquad (1)$$

where lambda is the wavelength of transmitted signal. Angle of arrival is found from the phase difference given in Eq. 2

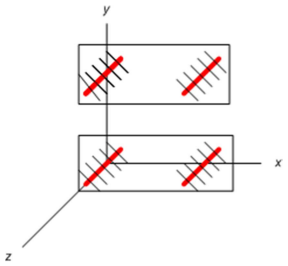
$$\theta = \sin^{-1}(\Delta\phi \ \lambda \ / \ (2\pi d)) \qquad (2)$$

We can combine the signals from 2 antennas at same axis. Combining the sensor output as



From Eq. (1)

$$phase\ diff = \Delta x = 2\pi dx sin\theta cos\phi / \lambda \quad (3)$$



Similarly

$$phase\ diff = \Delta y = 2\pi dy sin\theta sin\phi / \lambda \quad (4)$$

Now we can solve Eq. (3) and (4) to find θ and ϕ . Rearranging both equations as

$$sin\theta cos\phi = \Delta y\lambda / 2\pi dx \quad (5)$$

$$sin\theta sin\phi = \Delta x\lambda / 2\pi dy \quad (6)$$

Now from Eq. 5 $sin\theta = \Delta y\lambda / 2\pi dx cos\phi$

Putting above relation in Eq. (6)

$$sin\phi / cos\phi = \Delta xdx / \Delta ydy$$

$$\Rightarrow Azim = \phi = tan^{-1}(\Delta xdx / \Delta ydy) \quad (7)$$

Now put ϕ in Eq. (5) to find elevation θ. According to Eq. (6) and (7), if we know the phase differences Δx and Δy, we can find the azimuth and elevation angles and thus can localize the target. Let the data from antennas in Fig. 16 is $1 \Rightarrow x1$, $2 \Rightarrow x2$, $3 \Rightarrow x3$, $4 \Rightarrow x4$.Combining the data from 1,3 and 2,4

D1=x1+x3 , D2=x2+x4

The phase of D1 and D2 is found by taking the FFT and then finding phase. The phase difference becomes

$$\Delta x = phase\left(fft\left(D1\right)\right) - phase\left(fft\left(D2\right)\right)$$

Now, combining data from 1,2 and 3,4

D3=x1+x2, D4=x3+x4

Similarly

$$\Delta y = phase(fft(D3)) - phase(fft(D4))$$

Finally Δx and Δy are used to find azimuth and elevation.

Proposed architecture for direction finding system using phase difference method discussed above is shown in Fig. 9

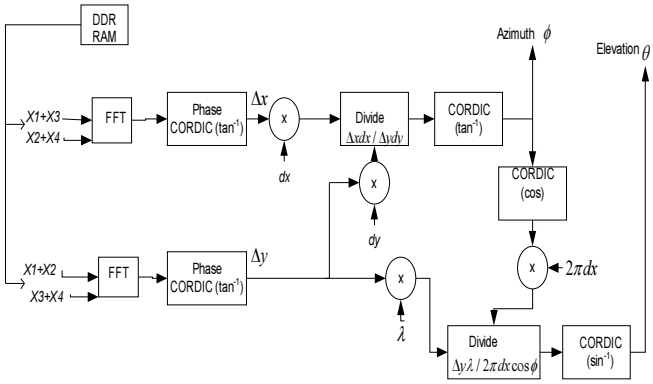


Figure 9. Architecture for Direction finding

4. Conclusions. Pulse Doppler Radar signal processor for air surveillance is simulated using MATLAB and then FPGA is used for testing the algorithm on processor. The design approach is explained with hardware/software partition and system block diagram. Antenna array system for direction finding was presented with its architecture. The results for simulation and hardware show that our system is working fine in presence of noisy signals.

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